TRANSNATIONAL ACCESS
USER PROJECT FACT SHEET

USER PROJECT	
Acronym	**FT Operation**
Title	**Fault-Tolerant Operation of a Wind Turbine with Control Hardware-in-the-Loop Tests**
ERIGrid Reference	**01.005-2016**
TA Call No.	**654113**

HOST RESEARCH INFRASTRUCTURE			
Name	**ICCS-NTUA**		
Country	**Greece**		
Start date	**06/06/2017**	**Nº of Access days**	**15**
End date	**26/06/2017**	**Nº of Stay days**	**21**

USER GROUP	
Name (Leader)	**Kai Ni**
Organization (Leader)	**University of Liverpool**
Country (Leader)	**United Kingdom**

1. USER PROJECT SUMMARY (objectives, set-up, methodology, approach, motivation)

1) Objectives: Validate the proposed control algorithms in control hardware-in-the-loop (CHIL) for the fault-tolerant four-switch three-phase (FSTP) converters in doubly-fed induction generator-based wind turbines (DFIG-WT) on a digital real-time simulator (DRTS).
2) Set-up: The set-up of the experiment is illustrated in Fig. 1, with the back-to-back power converter circuit simulated in DRTS and the control algorithms in CHIL.

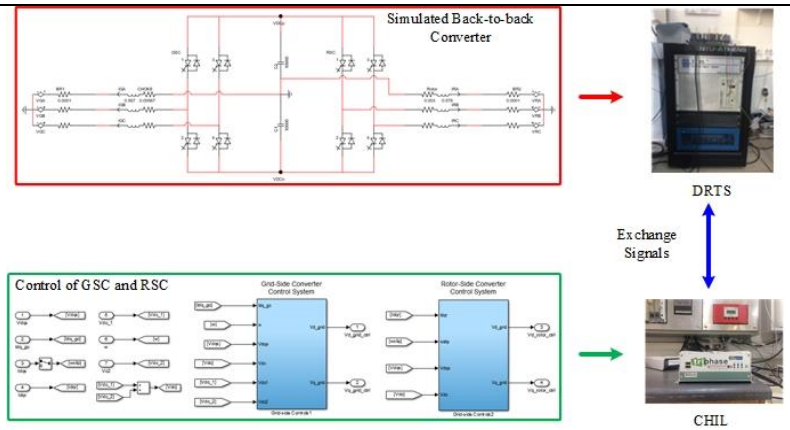

Fig. 1. Experimental platform set-up

3) Methodology: When one of the six power switches in the grid-side converter (GSC) or rotor-side converter (RSC) breaks down, the faulty bridge arm is isolated by connecting the corresponding phase to the midpoint of DC-bus to form FSTP topology.
4) Approach: The duty ratios of the switches in the two healthy bridge arms can be calculated according to the relationships among the basic voltage vectors used, and then the corresponding switching signals can be generated. Balance between the voltages on the two DC-link capacitors can be achieved by the proposed control algorithm for suppressing the voltage difference.
5) Motivation: With the fast development of wind energy, the reliability of wind turbines is becoming more and more important. As the failure rate of the semiconductor switches in the converters of DFIG-WTs, which take around 50% of the wind energy market, is relatively high, it is necessary to improve the fault-tolerant ability of these converters. Considering minimized number of switches, condition and switching losses, and simple structure, FSTP topology is used.

2. MAIN ACHIEVEMENTS (results, conclusions, lessons learned)

1) Results: The validity of FSTP topology-based back-to-back converter is demonstrated on DRTS with the control algorithms operated in CHIL. Detailed explanation will be given in the report.
2) Conclusions: a) More realistic situations are applied by employing CHIL set-up and DRTS.
b) The tracking performance of the controllers is validated.
3) Lessons Learned: a) Establish power circuits in RSCAD and run them on DRTS. b) Addressing issues that emerge from the appliance of the control algorithm in realistic conditions (noise, time delays). c) Implement and verify the control algorithms in CHIL. d) The techniques of tuning the controller gains in Matlab.

3. PLANNED DISSEMINATION OF RESULTS (journals, conferences, others)

1 journal article and 1 conference paper will be published based on the achievements.
In addition, the results of this proposed research will be involved in the training process for the undergraduate and MSC projects in University of Liverpool (UoL).