SIMPLE AC POWER SYSTEM

This Tutorial Manual builds on the basic steps required to construct and run an RTDS simulation case as outlined in the previous Chapter. A simple AC power system circuit is constructed and simulated here. Important aspects that are outlined herein include;

A. single line diagram drawing

B. preparation of transmission line data using the RSCAD/TïLine module

C. introduction of a fault branch

D. sending a signal to an analogue output channel

2.1 INTERïCONNECTING SINGLE LINE DIAGRAM COMPONENTS

When interconnecting power system components in singleïline drawing mode it is important that enough space is left between components so that there is room to display the component's three phase view without overlapping neighbouring components. To help in spacing the components in single line mode a light gray box surrounds each component. This box is only visible when drawing in single line mode. Neighbouring components should be placed so that their light gray boxes do not overlap. Figure 2.1 shows the connection of generator and transmission line components to a bus in single line diagram mode.

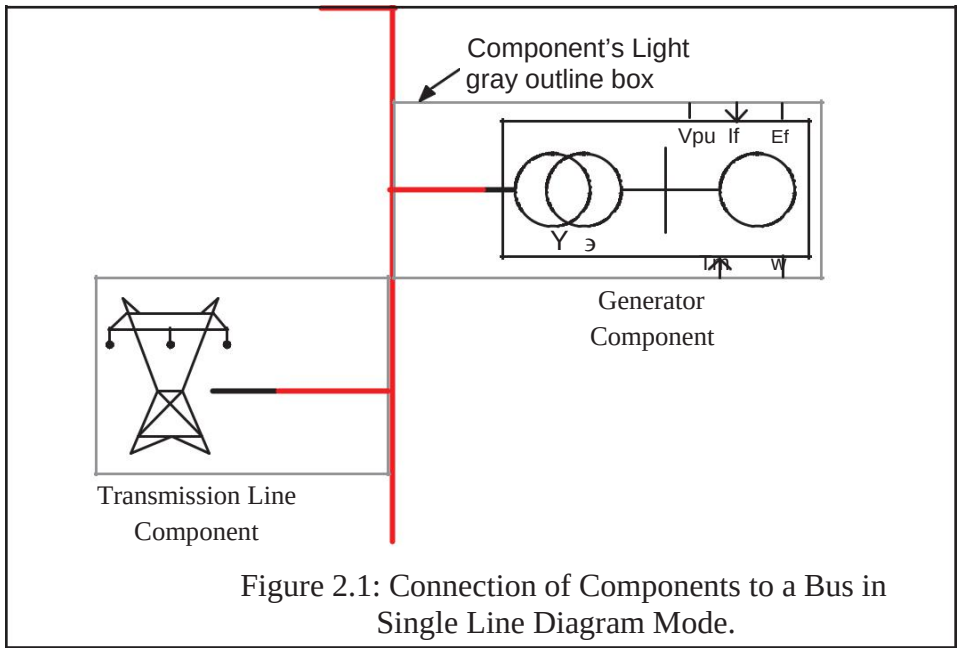


Figure 2.1: Connection of Components to a Bus in Single Line Diagram Mode.

Bus component icons may be directly connected when placed in single line diagram mode. Bus over connections are automatically made to ensure that phase A does not connect to phases B and C. These connections can be seen by switching back to 3 Phase mode. Since bus connections may be expanded to 3 Phase mode, parallel bus connections must be placed at least two connection points apart. An attempt to place single line bus components too close together results in a “bounds error” and the component is not placed. Figure 2.2 shows the location of valid bus connection points.

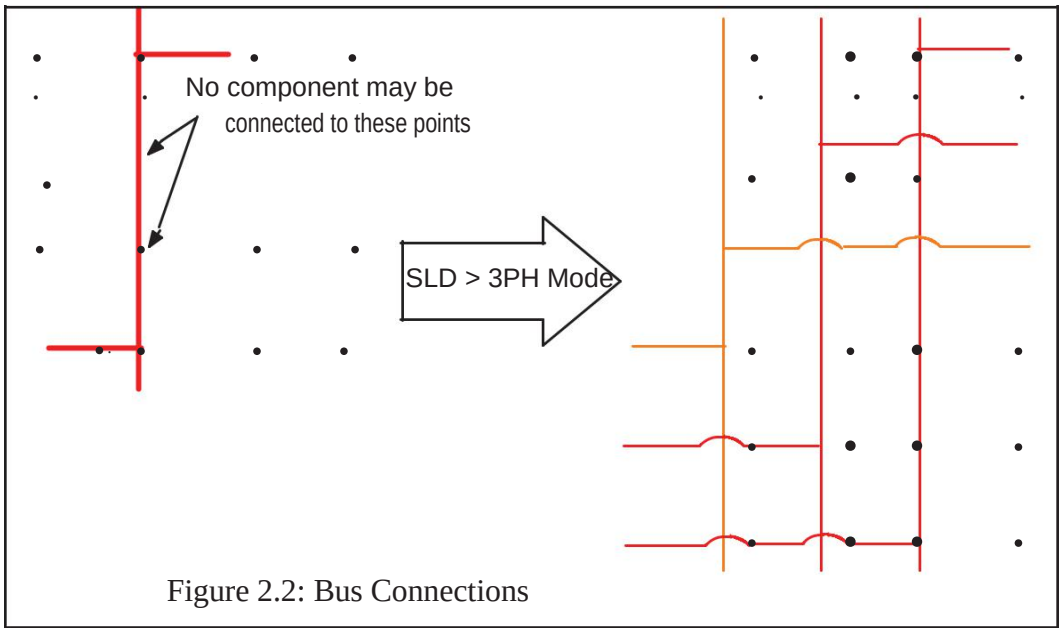


Figure 2.2: Bus Connections

2.2 POWER SYSTEM MODEL

The simple power system circuit used as the example is shown in Figure 2.3. The circuit is shown in single line diagram mode. The power system consists of a source model connected to a simple R // L load through a transmission line. The circuit is created using single line diagram components from the Power System library.

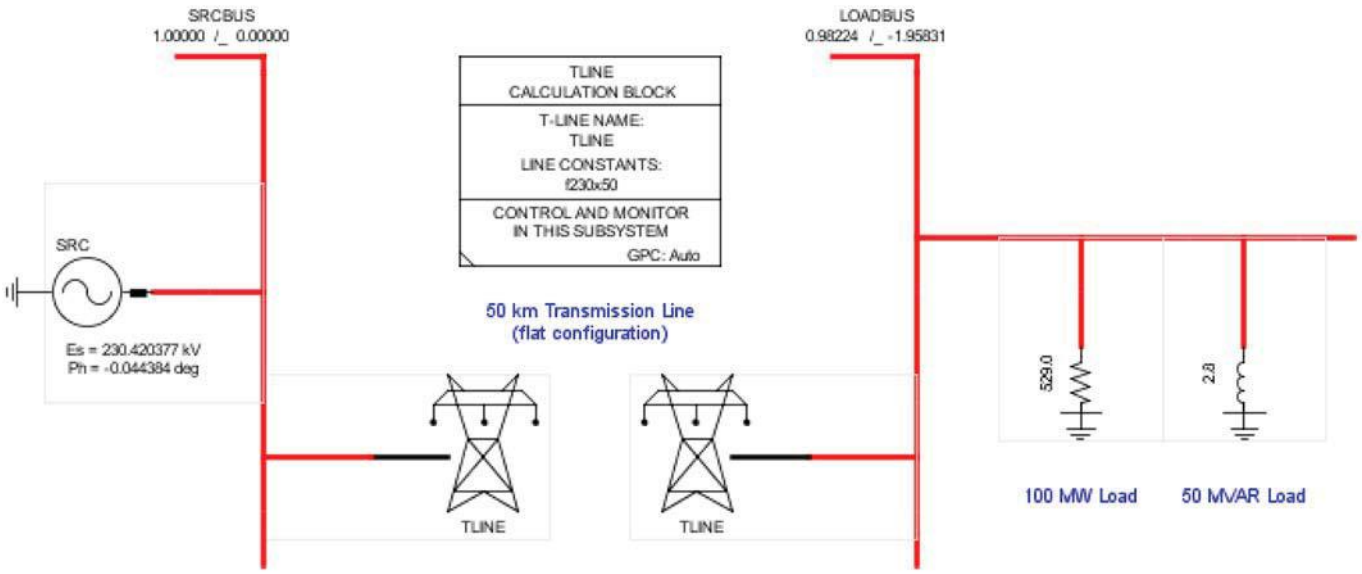


Figure 2.3 Simple AC Power System

SOURCE MODEL

A source model is often used to represent some portion of the power system in a simplified way. The source model generates a 3 phase power system frequency sine wave behind an impedance. Since the sine wave's magnitude, phase and frequency do not change in response to changes in the system to which it is connected, the source model is sometimes referred to as an "infinite source". Infinite because any amount of real and reactive power would have to be generated to maintain a bus voltage at a given setïpoint irrespective of system conditions.

If the source impedance is set to a very low value relative to the base impedance of the system at the bus to which it is connected, then the bus voltage to which the source is connected will also remain constant.

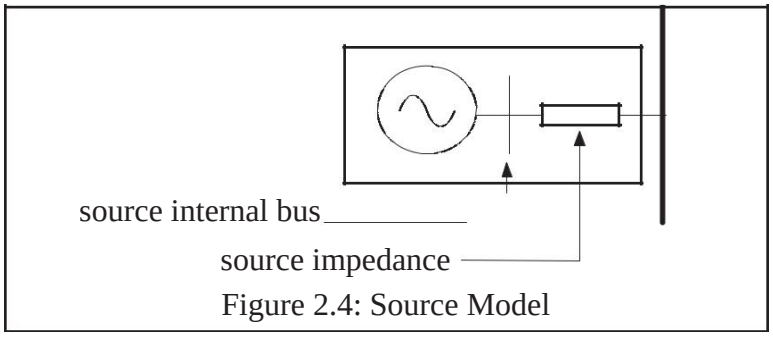


Figure 2.4: Source Model

A more realistic representation is one where the source impedance is chosen based on the short circuit capacity of the system which the source model is representing.

Care should be taken when specifying impedance values in ohms. The value of impedance in ohms should always be considered relative to the base impedance of

the system where the component is being placed. A 1: resistor on the 230 kV side of a transformer may be considered small for a base MVA of 100, but a 1: resistor placed on the 13.8 kV side of a transformer with the same base MVA is quite large.

on the 230 kV side 1 pu impedance= 230*230/100= 529 :
on the 13.8 kV side 1 pu impedance= 13.8*13.8/100= 1.9 :

hence a 1 : resistor on the 230 kV side corresponds to 0.00189 pu
a 1 : resistor on the 13.8 kV side corresponds to 0.525 pu

For the example case here, the source model impedance can be set to 1.0 : purely resistive source.

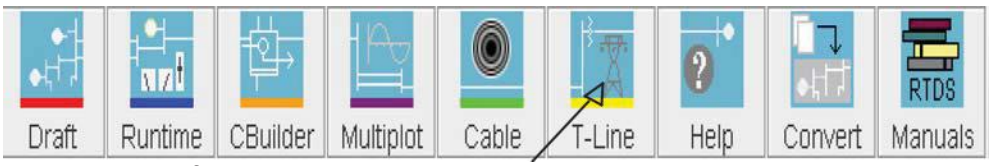
If there is at least one source model anywhere in the user's power system circuit then all generators connected to that circuit will operate at exactly the source's specified power system frequency in steadyïstate. In the case where the power system circuit includes no source models, only generators, then the generator frequency may not be at exactly nominal frequency in steadyïstate. Although all generators will run at the same frequency, the value of that frequency will be determined by the droop characteristic of the generator speed governor and the loading conditions of the system.

TRANSMISSION LINE DATA

Transmission lines are generally modelled using travelling wave algorithms within the RTDS. To model multiïconductor transmission lines using the travelling wave algorithm, data such as the line's modal characteristic impedances, travel times and transformation matrix must be determined. A separate RSCAD software module is available to generate the required data from line parameters more commonly available.

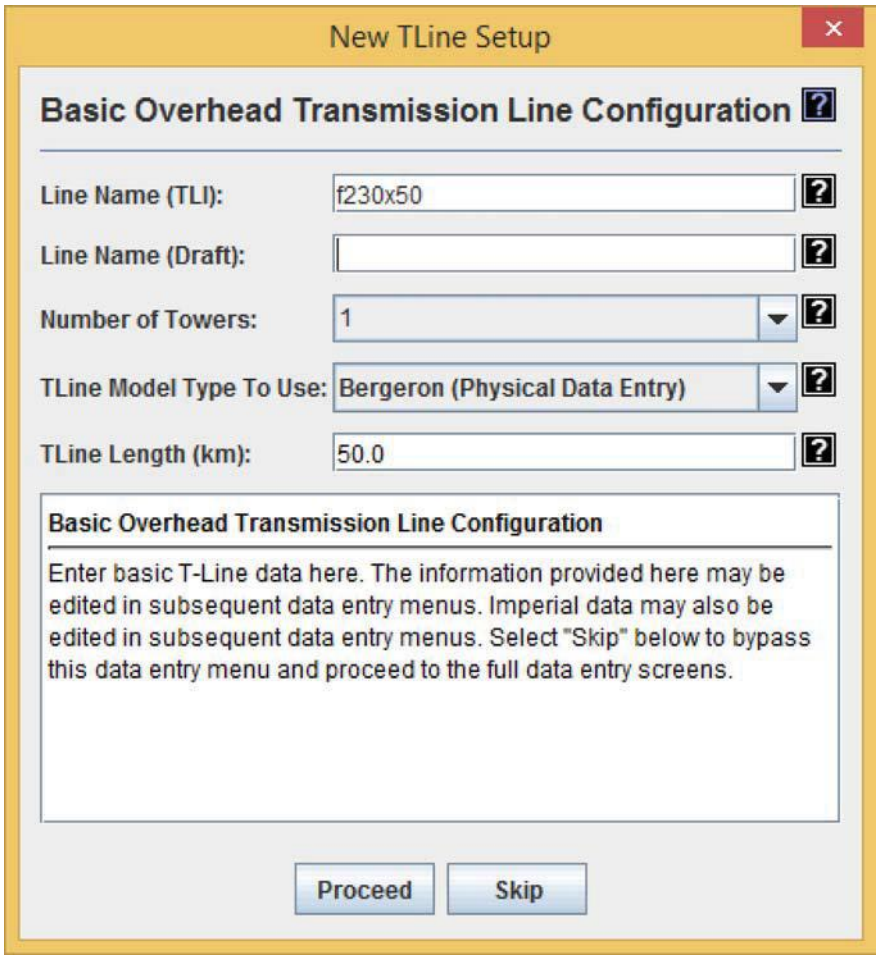
An exception to the use of the travelling wave algorithm is when the line travel time is shorter than the simulation timeïstep. In this case the line is represented using lumped RïLïCcomponents arranged as a PIï Circuit. With a timeïstep of 50ΠIs lines shorter than 15 km may be modelled using a single PIïSection.

Travelling wave transmission line components available in RSCAD/Draft require that the user specify the name of the file containing the transmission line data. The RSCAD software module known as TïLINE is used to generate the required tline data file. To start RSCAD/TïLine, select the TïLine icon from the RSCAD/FileManager tool bar.



Left Click to start RSCAD/TïLine

Select the "TLine Version 2.0 (2014)" radio button from the options menu that appears, then click OK. Select the "New File" radio button, then click OK. The following window will appear:



New Transmission Line Setup

As the description says, this infomation can be entered in subsequent data entry menus. Enter the data and click “Proceed” or leave it blank and click “Skip.” Clicking on [?] will give more information about each data entry.

Transmission line data may be entered as physical characteristics of the conductors and their location relative to each other and earth, or alternatively as positive and zero sequence impedances. The line options are found on the left side of the window.

Model: Bergeron or Frequency Dependent

The Bergeron line model represents the line’s characteristic impedance and travel time at only a single frequency (the frequency specified by the Low Frequency parameter under the Frequency Data Section in the options menu). With this model the increased damping of higher frequencies due to the *skin effect* is not represented.

The Frequency dependent line model uses curve fitting techniques to represent the frequency dependence of the line’s parameters. Frequency dependent damping is represented when using this model.

For the example case:

Line Options
Model: Bergeron (Physical Data Entry)
Units: Metric

Line Information
Line Length: 50.0
Ground Resistivity: 100.0

Frequency Data
Low Frequency 60.0

Tower & Right of Way Data, Conductor Data and Ground Wire Data entry is done by left clicking the appropriate tab near the top of the window. Figures 2.5, 2.6 and 2.7 show line data used for the example case.

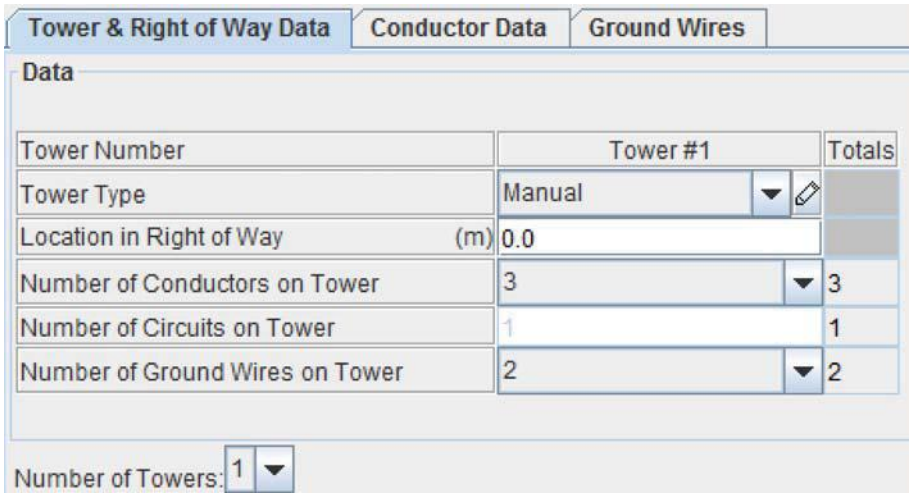


Figure 2.5: Tower & Right of Way Data

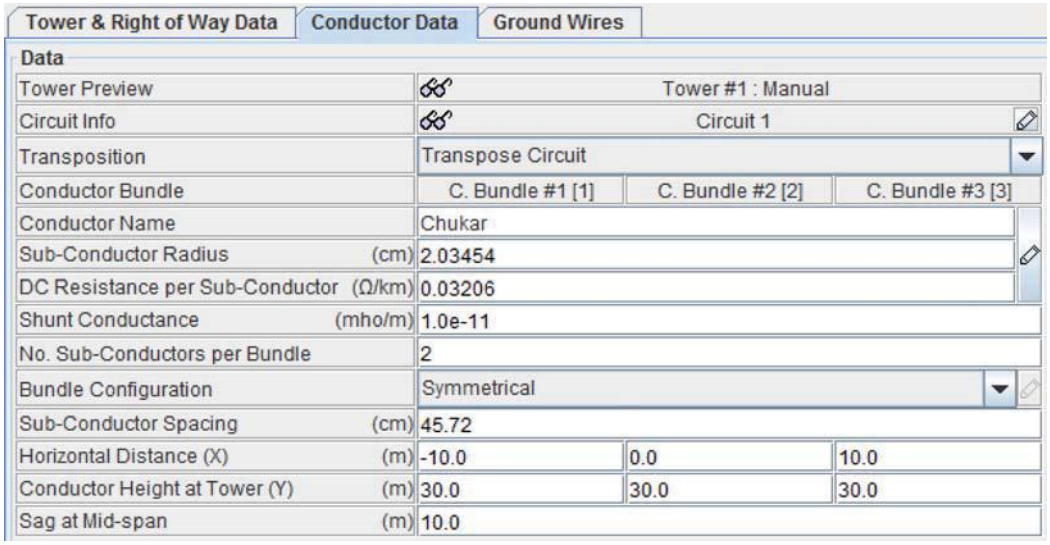


Figure 2.6: Conductor Data

Transposed: NonïTransposed or Transposed

For transmission lines whose phase conductors are not transposed or if the user places the transposition points manually in the RSCAD/Draft circuit, select NonïTransposed. In this mode the line's parameters will be unïbalanced.

Selecting Transposed results in the line being represented as perfectly symmetrical, equivalent to all conductors being equally spaced from each other and from ground.

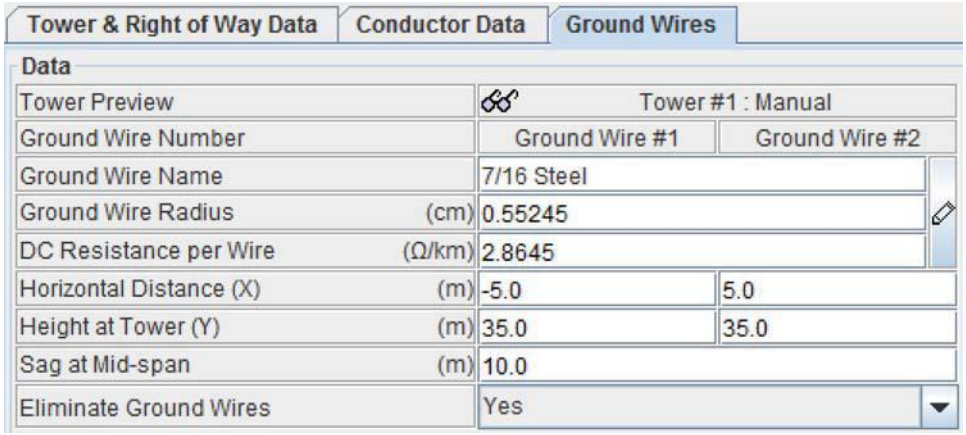


Figure 2.7: Ground Wire Data

Note that the sag at midspan parameter for both the conductor and ground wire data is measured from the conductor and not from ground. Thus, a conductor whose height above ground at the tower is 30m and has a specified sag at midspan of 10m will droop to 20m above the ground.

The number of subïconductors, sub ïconductor radius and subïconductor spacing refer to the conductors comprising a single phase. For EHV and UHV transmission systems, often more than one conductor per phase is used. Figure 2.8 shows the physical arrangement of a 4 subïconductorbundle and the data required for the tïline program.

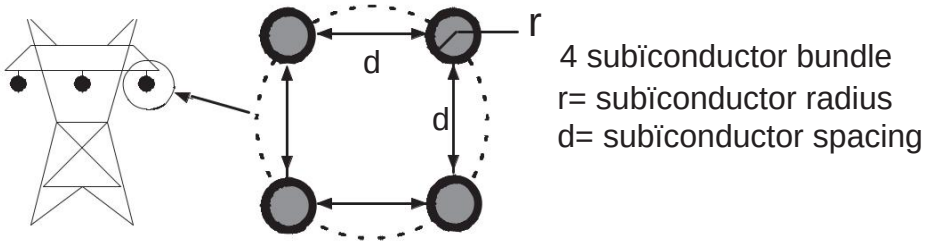


Figure 2.8: SubïConductor Bundle

Once the options have been selected and the conductor and ground wire data have been entered, the compile option is selected from the TïLine tool bar.

The compile procedure computes the necessary parameters and stores them in a user specified base file name. The base file name is appended with ".tlo". Note that the tline data file should be stored in the same PROJECTï>CASE directory in which the user's simulation case is being prepared. The base file name chosen here is entered as the tïline data file name (Dnm1 parameter) in the EDIT menu for the transmission line component in RSCAD/Draft. In the same EDIT parameters menu, change "Read line constants from:" (rdData parameter) to "tlo/clo."

PASSIVE LOAD

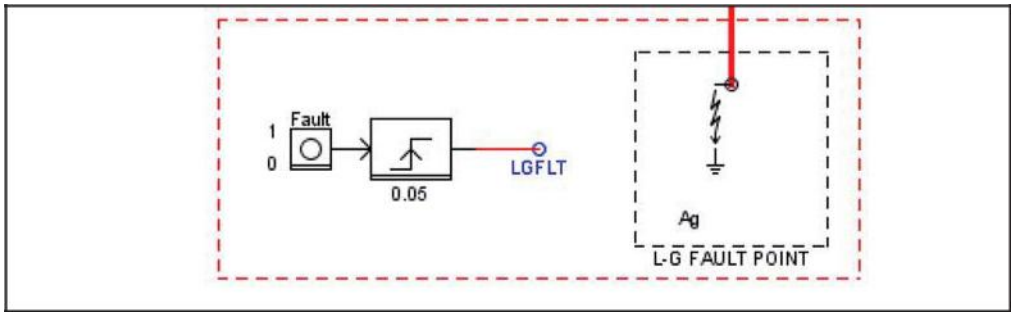
Loads are the *raison d'être* of power systems and their representation in simulation cases is often overïlooked. In their simplest form loads may be represented by fixed shunt passive elements. Resistive, inductive and capacitive shunt branches may be placed at a bus to represent real and reactive loads. Other components which may be used to model loads include ï

Source model with fixed magnitude and phase
Induction machine model
Static load model
Dynamic load model

FAULT BRANCH & FAULT CONTROL

A fault branch may be connected to a bus in order to simulate a short circuit at that bus. The fault branch consists of a switch whose open resistance is very large and whose closed resistance is specified by the user. The type of fault, lineïground or lineïline, is specified by the 'Type' parameter in the fault component CONFIGURATION menu. For a Lineï Gnd fault type, the user may select which phases will include a fault branch in the LïG PARAMETERS menu.

Control of the fault initiation and removal may be done using control components. Control components can be found in the Controls library tab. The most simple arrangement is to use the pulse generator control function and a pushïbutton. The pulse width specified for the pulse generator function determines the fault duration.



Signal names can be given to control component inputs and outputs using wirelabels. The signal name given to the pulse generator output must be the same as that specified for signal name to control the fault branch (Asig/Bsig/Csig parameters for the Fault Branch Data in the fault component menu). The value of the pulse must correspond to the value for the active bit number specified for the fault branch. For example, if the “Abit” parameter is set to 1 for an A Phase ï Ground Fault Branch then the “OT” parameter for the pulse generator function block should also be set to 1. Since the pulse output is specified as an integer value and the active bit as a bit number, the integer value must be computed as $2^{(bitî1)}$. A bit number of 3 corresponds to an integer value of $2^{(3î1)}$ = 4. Multiple fault branches may be controlled from the same control signal by specifying the same Signal Name and Active bit for each fault branch.

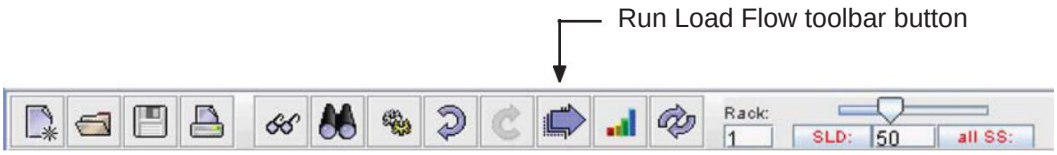
2.3 RUNNING THE DRAFT EMBEDDED LOAD FLOW PROGRAM

It is possible to run a load flow for the power system circuit from RSCAD/Draft. The load flow computes the initial voltage magnitude and angle for each bus in the circuit. Components such as sources and generators are also initialized. By running the load flow it is possible to start the RTDS simulation case in a quasi steadyïstatecondition. For simulation cases that contain numerous generators the initialization performed by the load flow will help in arriving at a stable operating point.

In preparation to run the load flow, the bus type parameter and rated voltage must be specified within the bus label component for ***all*** buses. Buses may be specified as slack (voltage magnitude and angle specified), PV (real power and voltage specified) or PQ (real and reactive power specified). One bus within the power system circuit must be specified as the slack bus. Buses to which generators are connected are typically identified as PV since the generator power and terminal voltage are regulated. If a bus to which a source model is connected exists in the user’s circuit it can be identified as the slack bus. Load buses are usually assigned as PQ buses.

In this example, the source bus should be specified as the slack bus with a rated voltage of 230 kV. The load bus should be specified as a PQ bus with a rated voltage of 230 kV. After entering the required information, the load flow can be run by left

clicking the load flow button from the RSCAD/Draft tool bar located above the drawing canvas.



A parameters menu will appear in which the user must provide the following data;

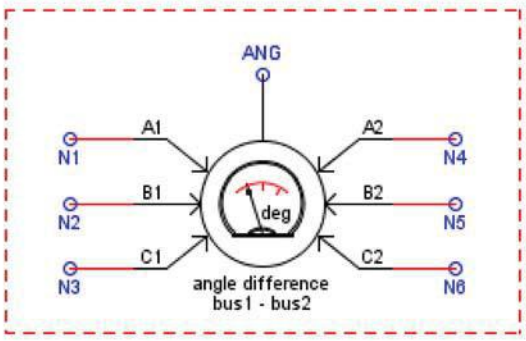
Base Frequency: The system's base frequency in Hz. (eg. 50.0 or 60.0)

Tolerence: The maximum allowable power misï match at a bus, specified in MVA. When all bus misï matches have fallen below the specified level the load flow solution is considered complete.

Once the load flow has completed, various parameters within the user's circuit will have been automatically initialized. Bus voltage magnitudes and angles computed from the load flow will be displayed over the bus component icons. The "AC Source Initial Power Output" parameters will also be initialized.

In order to run the case using parameters updated by the load flow, the user must compile the simulation case before proceeding to RSCAD/RunTime.

To check to see if the computed load flow matches the results of the simulation, the angle between the two buses can be measured using an angle difference meter as shown below. The angle difference meter can be found in the Controls library tab and can be added to the Draft circuit.



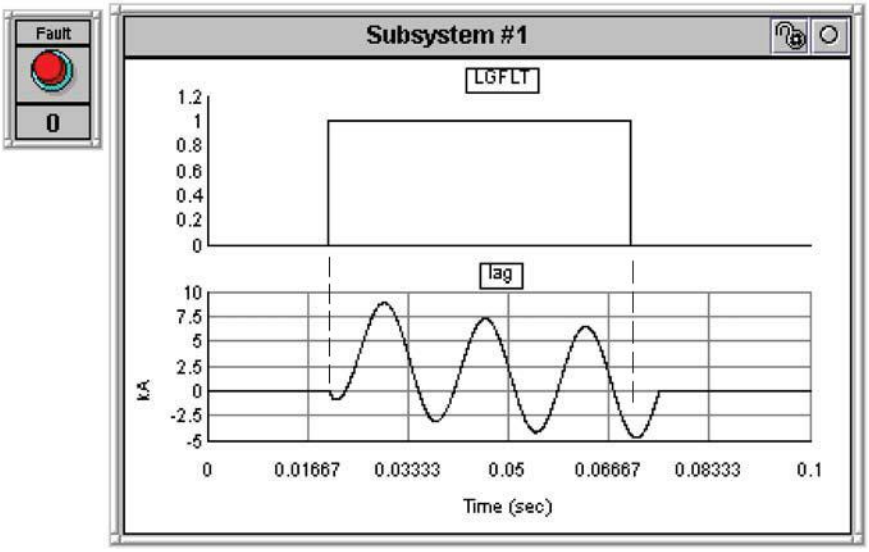
Note: Power system signals are referred to as electrical signals and control system signals are referred to as control signals. Electrical signals can be directly connected to control components using wire labels. In draft, monitored wire labels are blue in colour while unmonitored wire labels are green. An IMPORT/EXPORT component can also be used to export the node voltages from the power system circuit and import to a control component.

2.4 RUNNING THE SIMULATION CASE

To run the simulation, compile the circuit from RSCAD/Draft and then load the case into RSCAD/RunTime as outlined in Section 1.6. Meters and plots may be created to monitor various system quantities such as bus voltages, line currents etc.

In order to apply the fault the fault initiation push button must be created. Select the createï >pushbuttonoption from RSCAD/RunTime and then select the button named “Fault” from the Subsystem #1ï>CTLsï>Inputs section.

It is interesting to plot the output of the pulse generator “LGFLT” and the fault current on two grids within the same plot. Notice that the fault current changes immediately after the initiation of the fault by the “LGFLT” signal becoming ‘1’. However, the fault current does not extinguish until the first current zero subsequent to the “LGFLT” signal becoming ‘0’.



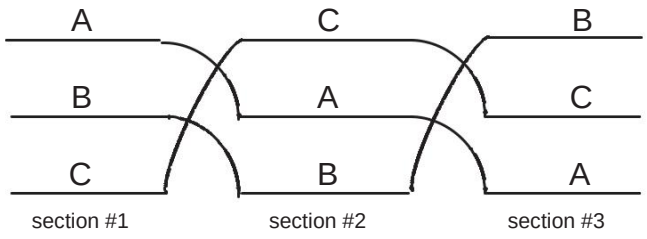
The fault branch will not open until the fault trigger signal is ‘0’ and the fault current passes through 0.0. The fault current threshold to remove the fault may be changed to a value other than 0.0 by setting the “Agholdi” parameter in the Ground Fault Branch Data submenu in the fault component. It is recommended that value be kept at 0.0 since opening the fault switch at a value other than 0.0 may result in a large voltage spike. If the fault current is flowing through an inductance and the fault switch is opened at a non current zero the voltage across the inductor will suddenly change by an amount L*di/dt.

TRANSMISSION LINE PHENOMENA

Although the simulation case documented here is quite simple, consisting only of a source, a transmission line and a load, many interesting power system phenomena may be observed.

Unbalance & Transposition

If “Transposition” in the transmission line is changed to “NoniTransposed” the transmission line currents in the simulation case are not symmetrical in steadyïstate. To accentuate the uniïbalance, the load at the receiving end may be removed. It can then be observed that the ‘B’ Phase current is approximately 10% higher than the ‘A’ and ‘C’ Phase currents. Long transmission lines are often transposed so as to balance the line currents. There are two ways to include transpostion into the RTDS simulation case. Firstly, transpostion may be modelled explicitly by dividing the transmission line into three sections of equal length. At the connection between section 1 and section 2 a single phase rotation is done. Phase A is moved from conductor 1 to conductor 2, Phase B from conductor 2 to conductor 3 and Phase C from conductor 3 to conductor 1. Another such rotation is done at the connection point between sections 2 and 3. With such a transposition scheme each phase will occupy the same length on conductor 1, conductor 2 and conductor 3. This approach requires the user to allocate 3 transmission line models and six extra nodes.



Explicit Transmission Line Transposition

The second method of including the effects of transposition is to select “Transpose Circuit” in the Conductor Data menu of the RSCAD/TïLine program. In this case the line may be modelled using one transmission line component. No intermediate nodes are needed.

In the case when multiple circuits are suspended from the same tower, transposition is done on a per circuit basis. This means that the A, B and C phases of each circuit are transposed. Transposition between circuits is not normally done. To transpose individual circuits when there is more than one circuit per tower, in the RSCAD/Tï Line Conductor Data menu set the Transposition option to “Transpose Circuit” for each circuit .

Ferranti Effect

The Ferranti effect refers to the rise in voltage that occurs along a transmission line whose receiving end is openïcircuit. With the 50 km line used in the example herein the Ferranti effect is very small. With no load connected to the receiving end of the line the bus voltage at the receiving end is 230.5 kV a rise of only 0.2%. However, if the line length is changed to 500 km the open circuit voltage at the receiving end of the line is approximately 285 kV an increase of some 24%. If losses are ignored the openïcircuit voltage at the receiving end of a balanced line is given as ï

$$V_{re} = V_{se} / \cos(0.0721 * \text{Len(km)})$$

$$V_{re} = 230.0 / \cos(0.0721 * 500) = 284.5 \text{ kV}$$

Shunt passive reactors are often used on long transmission lines to limit the Ferranti Effect.

It should be noted that the open circuit condition results in the highest receiving end voltage. As load is added to the receiving end the bus voltage is reduced, falling to 1 pu when the load equals a value referred to as the Surge Impedance Load (SIL). The voltage drops below the sending end voltage as the load is increased beyond the SIL.

Another interesting effect is that the term cos(0.0721*Len) becomes 0.0 when the length is equal to 90/0.0721= 1248 km. At a line length of 1248 km. the receiving end voltage becomes infinite.

Surge Impedance Loading (SIL)

A transmission line terminated with a resistance equal to the line's surge impedance (also referred to as characteristic impedance) will have a *flat* voltage profile. This means that the voltage everywhere along the line, including the receiving end terminal, will be equal to the sending end voltage. The Surge Impedance Load is defined as ï

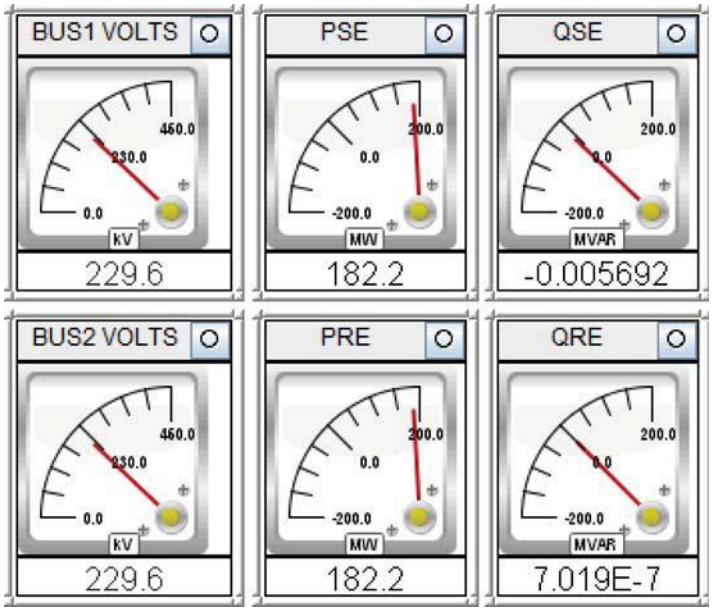
$$SIL = V^2 / Z_{surge}$$

The surge impedance of an overhead transmission line is determined by the physical characteristics of the line, particularly the spacing between phase conductors and conductor dimensions and is typically in the range of 200 ï 400 :.. The surge impedance is not dependent upon the line's length. A 3 phase line has zero, positive and negative sequence surge impedances. If the line is balanced then the positive and negative sequence surge impedances are equal.

A file named *filename*.out is produced whenever the compile option from RSCAD/TïLine is selected. The .out file is located in the same directory specified for storage of the line's .tli and .tlo file. The .out file contains information regarding the line's surge impedance. Under the heading "MODAL CHARACTERISTIC

IMPEDANCE VECTOR" the zero sequence, positive sequence and negative sequence surge impedances are listed.

To run the case documented here with a surge impedance load, change the line characteristics to ideally balanced, set the line's DC resistance to a very low value (Eg. 1.0eï 6 :/km), remove the inductive load and change the resistive load component to a value of 289.3328:. The receiving end voltage is now equal to the sending end voltage (ie. 230.0 kV) and the transmitted power is equal to the SIL. Note that the reactive power flow through the line is approximately 0.

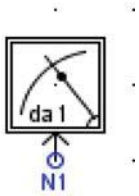


System Meters for SIL Terminated Line

2.5 SENDING A SIGNAL TO A FRONT PANEL ANALOGUE OUTPUT CHANNEL

As mentioned in Chapter 1, the RTDS hardware is continuously running with a very small timeïstep (typically 50 Πs) and it is not possible to collect all of the data continuously. To monitor data continuously during a simulation, signals can be monitored using a scope. A scope can be connected to an analogue output channel of the RTDS. The Draft circuit must be modified to specify *what* signal to send to *which* D/A channel and at *what* level. An analogue output channel control component can be used to send a signal to a D/A channel on the front panel of a processor card. Each processor has direct access to 12 analogue output channels. The analogue channel's output voltage range is +/ï 10 volts peak.

The control blocks shown below can be added to the circuit to send the voltage signal named 'N1' to an analogue output channel. Control components are located in the Controls library tab.



The analogue output component parameters are as follows;

DA ï The analogue output channel is specified here. Any of the twelve channels available on the processor may be used.

SC ï scale the input signal so that the specified value will result in an analogue output voltage of 5 volts peak. The scale value required is peak. In this example, setting the scale value to 187.89 will result in 5V peak out of the D/A channel.

SL ï Dynamic offset and scale sliders may be included (SL parameter). If enabled the user is able to create RSCAD/RunTime sliders to dynamically adjust the analogue output offset and scale. A RSCAD/RunTime switch may also be created which controls the LED associated with the analogue output channel. The LED can be turned on by the switch to help locate the analogue output port on the front of the RTDS.

Compiling the circuit generates a map file. The map file contains details on how the circuit has been allocated to the RTDS. In this example, the analogue output component has *not* been manually assigned a processor. Therefore the map file must be referenced to determine which processor the analogue output signal is available. To view the map file, select the view button available from the RSCAD/Draft toolbar. A box is displayed that allows the map file to be selected. The map file will be displayed in a text editor and the name of the analogue component can be found. For example,

```
RISC CONTROLS COMPONENTS(proc 1) --> RPC-GPC Card #1 Processor B
      RISC Pulse Generator (pulse width= 0.050000 sec.)
      RISC Angle Difference Meter (next 9 components)
      RISC 3 Phase --> A-B Transformation
      RISC 3 Phase --> A-B Transformation
      RISC MULTIPLICATION function
      RISC MULTIPLICATION function
      RISC Floating Point Summation + +
      RISC MULTIPLICATION function
      RISC MULTIPLICATION function
      RISC Floating Point Summation + -
      RISC ARCTAN2 Function
      RISC GPC Analogue Output (Channel #1)
```

The map file above shows that the signal will be available for monitoring on card #1 processor B channel #1. Note, the map file will vary based on different RTDS hardware configurations. Therefore, the analogue output component may not always

be assigned to card#1 processor B. A scope can be connected to this location on the RTDS and the N1 signal monitored after the simulation has been started.

Alternatively, the analogue output component can be manually assigned to a processor using the *Assign Control Processor* control block. The control processor number entered in each control component is a reference number. For example, all control components have a 'Proc' parameter that is used as a reference number;

Proc	Assigned Controls Processor	2	1	54

The *Assign Control Processor* control block requires the control processor reference number as input.

Assign Control Processor control block

All control components with control processor reference set to 2 will be assigned to the processor selected in the *Assign Control Processor* control block.

The front panel analogue output channels use 12 bit D/A's and do not include optical isolation. For high precision optically isolated analogue output, external analogue output cards are used such as a GTAO. Signals can be sent to a GTAO card using a GTAO control component in a similar manner.