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Technical Report TA User Project

Fault-Tolerant Operation of a Wind Turbine with Control Hardware-in-the-Loop Tests

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[Rev. 1]	Description of the fault-tolerant back-to-back converter in DFIG-WT, control algorithms and results obtained in ICCS-NTUA.	Kai Ni, University of Liverpool	17.07.2017
[Rev. 2]	Review and additional inputs	Dimitris Lagos, ICCS-NTUA	25.07.2017
[Rev. 3]	Further modifications	Kai Ni, University of Liverpool	25.07.2017

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Abbreviations

APF	Active Power Filter
BLACM	Brushless AC Machine
BLDCM	Brushless DC Machine
CHIL	Control Hardware-in-the-Loop
DFIG	Doubly-Fed Induction Generator
DFIG-WT	Doubly-Fed Induction Generator-Based Wind Turbine
DRTS	Digital Real-Time Simulator
FSTP	Four-Switch Three-Phase
GSC	Grid-Side Converter
IM	Induction Machine
RSC	Rotor-Side Converter
SSTP	Six-Switch Three-Phase
SVPWM	Space Vector Pulse Width Modulation
PLL	Phase Locked Loop
PMM	Permanent Magnet Machine
PWM	Pulse Width Modulation
WECS	Wind Energy Conversion System
WT	Wind Turbine

Executive Summary

With the rapid development of WECSs, especially for offshore ones, wind energy is taking the leading status in the renewable energy market. Owing to its importance, the reliability of WTs is one of the most significant aspects to be considered. Around half of the wind energy market is dominated by DFIG-WTs. Since breakdown of the fragile semiconductor devices in the back-to-back converters in DFIG-WTs usually leads to disconnection of WTs from the grid, the fault-tolerant ability of these converters are to be increased. In this project, FSTP topology is employed for the cases when one of the bridge arms in GSC or RSC is open-circuited, so that redundant bridge arms are not required. To validate the proposed control strategies used in practical cases, experimental verifications are carried out by simulating the power circuit in DRTS with the control algorithms performed in CHIL.

1 General Information of the User Project

User Project Title: Fault-Tolerant Operation of a Wind Turbine with Control Hardware-in-the-Loop Tests
User Project Acronym: FT Operation of a WT with CHIL Tests
Host Infrastructure: ICCS-NTUA
Access Period: 06/06/2017 – 26/06/2017
User Group Members: Kai Ni

2 Research Motivation

Wind energy is a promising renewable resource and it is estimated that by 2050 wind power will account for 15-18% of the total power generated all over the world [1]. While the fluctuation of wind speed increases the probability of fault. When faults occur in a wind turbine, the traditional way is to cut the turbine off the grid to avoid subsequent problems. This method is not applicable in the future as wind will be one of the main power sources, and the strike of WTs is not permitted. Especially for offshore wind turbines, access is limited for maintenance due to bad weather conditions and the fee for maintenance is high. In this case, the faulty WT can stop working for weeks, which causes a large amount of power losses. As the proportion of offshore wind farms is dramatically increasing in the EU recently, a practical solution should be proposed. To solve this problem, fault-tolerant ability of WTs should be improved, and then continuous power supply can be kept. Nowadays, power electronic converters are playing important roles in power systems, and breakdown of power electronic switches in the converters is one of the main causes of faults (21% of the total cases [2]). A fault-tolerant converter topology called FSTP topology is presented to solve this problem.

2.1 Objectives

1) Use FSTP converter topology to make DFIG-WT continuously operate after short circuit happens in one of the bridge arms.
2) Minimize the side effects induced by using FSTP topology by using the proposed control algorithm.
3) Validate the proposed control algorithms in CHIL setup for the fault-tolerant FSTP converters in DFIG-WT on DRTS.

2.2 Scope

As most of the DFIG-WTs on the market are now approaching the end of their lifetime, the possibility of faults occurring in the respective components increases a lot. For the semiconductor devices in the back-to-back converter of DFIG-WT, the failure rate reaches 21% [2]. Especially for offshore WTs, maintenance is seldom taken due to extremely high maintenance cost and terrible weather, and the faulty WTs may stop working for a long period of time, resulting in huge electricity losses and cost. With the proposed fault-tolerant converter topology, continuous operation of DFIG-WT can be kept when one of the switches in GSC or RSC breaks down to form an open circuit, and disconnection from the grid can be avoided. Under this situation, power is constantly supplied to the grid without deteriorating the overall quality. The proposed topology and control algorithms are verified in experiments in this project to demonstrate the feasibility.

3 State-of-the-Art/State-of-Technology

FSTP converter topology has been applied in different applications such as IMs [3-7], BLDCMs/BLACMs [8-9], PMMs [10-13] and APFs [14-15].
In [16] the modelling, modulation and control of FSTP inverter was investigated in detail. A simplified SVPWM technique was selected, where sector identification and complex trigonometric calculations are not required. Assume phase A is connected to the midpoint of DC-bus after the fault, the allocation of basic voltage vectors is displayed in Figure 1.

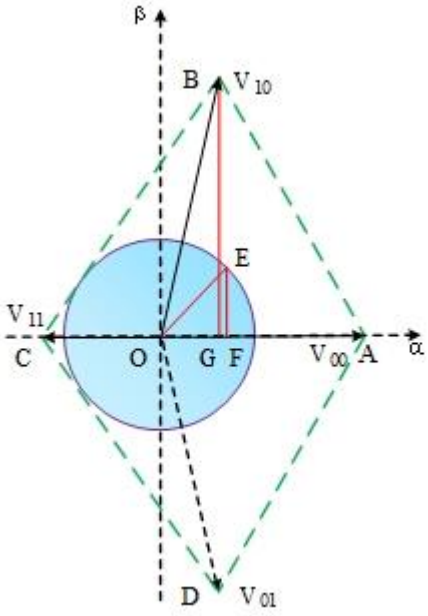


Figure 1. Allocation of the basic voltage vectors

Take FSTP GSC as an example, the reference values for the three-phase AC voltages are expressed as shown below:

$$\begin{cases} v_{AN\_ref} = V_m \cos(\theta_s) \\ v_{BN\_ref} = V_m \cos(\theta_s - \frac{2\pi}{3}) \\ v_{CN\_ref} = V_m \cos(\theta_s + \frac{2\pi}{3}) \end{cases} \quad (1)$$

OA, *OB*, *OC* and *OD* represent the four basic voltage vectors V_{00}, V_{10}, V_{11} and V_{01} respectively, where 0 means the upper switch in a bridge arm is off and the lower switch is on, while 1 denotes the opposite situation. In this case, *OE* is the reference voltage vector, and its components on α and β axes are *OF* and *EF* respectively. If *OA*, *OB* and *OC* are used for synthesizing *OE*, then the basic voltage vectors to be used are V_{00}, V_{10} and V_{11}. In addition, the time distributed to the vector V_{11} counteracts part of the time used for V_{00} which forms the equivalent zero vector. *OG* and *BG* are separately α and β components of *OB*, which is the vector V_{10}. Considering the situation in a switching period, the following relationships can be derived:

$$\begin{cases} OF = OA \times d_{00} - OC \times d_{11} + OG \times d_{10} \\ EF = BG \times d_{10} / \sqrt{3} \\ 1 = d_{00} + d_{10} + d_{11} \end{cases} \quad (2)$$

where d_{00}, d_{10} and d_{11} represent the duty ratios for V_{00}, V_{10} and V_{11} respectively. The values of *OF* and *EF* can be obtained as

$$\begin{cases} OF = v_{AN\_ref} \\ EF = \dfrac{v_{BN\_ref} - v_{CN\_ref}}{\sqrt{3}} \end{cases} \tag{3}$$

By combining (2) and (3), the duty ratio for each basic voltage vector is derived, and then the duty ratios for the two remaining bridge arms are calculated. Based on the conclusions obtained in [16] and double check by the authors, the results of the duty ratios in the two bridge arms d_b and d_c do not change with variations of either the sector or modulation method.

$$\begin{cases} d_b = \dfrac{V_{C2} - v_{AN\_ref} + v_{BN\_ref}}{V_{dc}} \\ d_c = \dfrac{V_{C2} - v_{AN\_ref} + v_{CN\_ref}}{V_{dc}} \end{cases} \tag{4}$$

The switching signals for the four switches can be derived by comparing the duty ratio values with a triangle waveform.

4 Executed Tests and Experiments

In this project, the FSTP GSC and RSC are respectively established in the DRTS software called RSCAD. The proposed control algorithms for these fault-tolerant converters are uploaded to a hardware controller in order to verify their operation under a CHIL setup.
The measurements of the power system are provided by the DRTS to the hardware controller. The hardware controller obtains the measurements and provides the control signals for the FSTP GSC and RSC to the DRTS. The performance of the FSTP GSC regarding the DC-bus voltage, three-phase grid currents and output power factor is investigated. Also, the effects of controlling the active and reactive power with FSTP RSC are researched.

4.1 Test Plan

The test plan can be divided into the following points:
(1) Test the performance of FSTP GSC without including DC-link capacitor voltage deviation suppression control.
(2) Test the performance of FSTP GSC with DC-link capacitor voltage deviation suppression control.
(3) Test the performance of FSTP RSC.

4.2 Standards, Procedures, and Methodology

Here are the procedures for the experiment:
(1) Establish the power converter circuit in RSCAD and obtain the output signals to CHIL.
(2) Figure out the principles of the proposed control algorithms.
(3) Calculate the scaling of the measurements and connect DRTS and CHIL to the network.
(4) Implement the proposed control strategy for FSTP GSC without including DC-link capacitor voltage deviation suppression control.
(5) Tune the controller gains, damping ratio, etc. to make the controllers work properly.
(6) After adding the DC-link capacitor voltage deviation suppression control into the GSC control algorithm, repeat step (5) again.
(7) Obtain and save the results.
(8) Implement the proposed control strategy for FSTP RSC.
(9) Repeat step (5).
(10) Obtain and save the results.

4.3 Test Set-up(s)

4.3.1. Implementation Details
The experimental platform setup is illustrated in Figure 2, where the simulated back-to-back converter power circuit is established in DRTS software with the mathematical equations calculated in DRTS, and the proposed control strategies are implemented in Matlab/Simulink and uploaded to a target computer that is interfaced with DRTS in the form of analog signals.

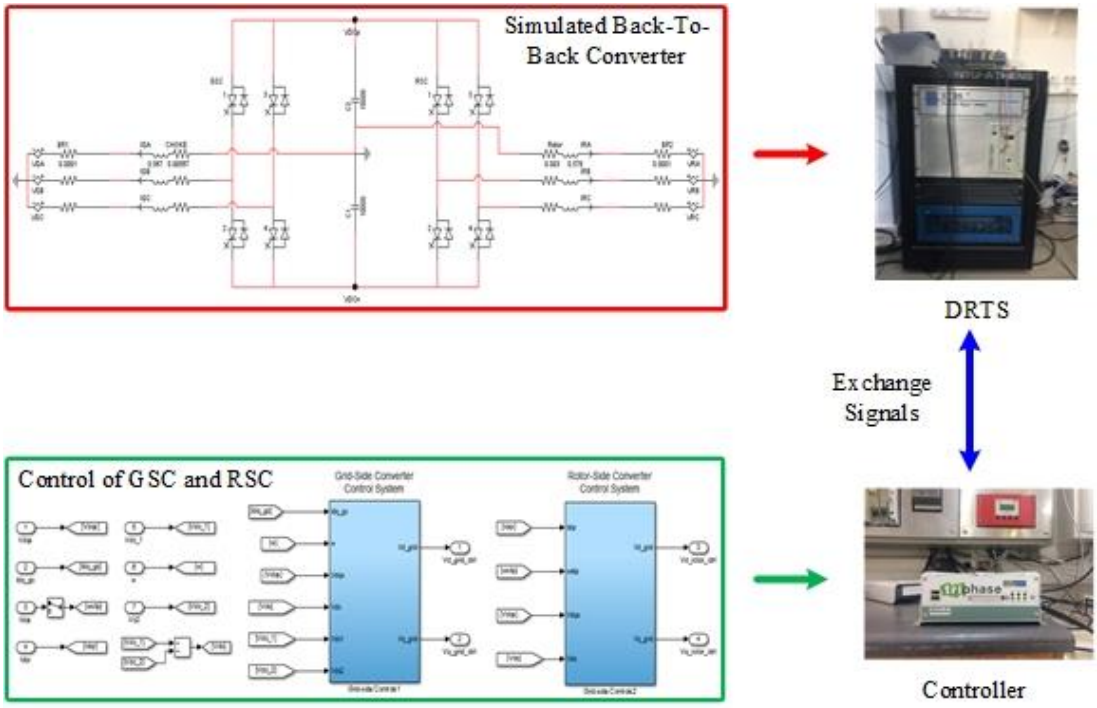


Figure 2. Experimental Platform Setup

4.3.2. Equipment and Communications Used

During the test, CHIL setup is used to simulate the control algorithms in almost actual situations, and DRTS is employed for simulating the power converter circuit. Signal exchange is achieved between DRTS and the controller.

4.3.3. Control Strategy

In terms of the control strategies, the upper and lower DC-link capacitor voltages should be measured separately according to the SVPWM technique mentioned above. With the assumption that the grid voltage source is balanced and not distorted, the three-phase grid voltage signals are captured by voltage sensors. The three-phase grid-side and rotor-side reference voltage signals v_{gabc_ref} and v_{rabc_ref} are obtained to generate the switching signals for the FSTP GSC and RSC. The control block diagram for the post-fault DFIG-WT is illustrated in Figure 3.

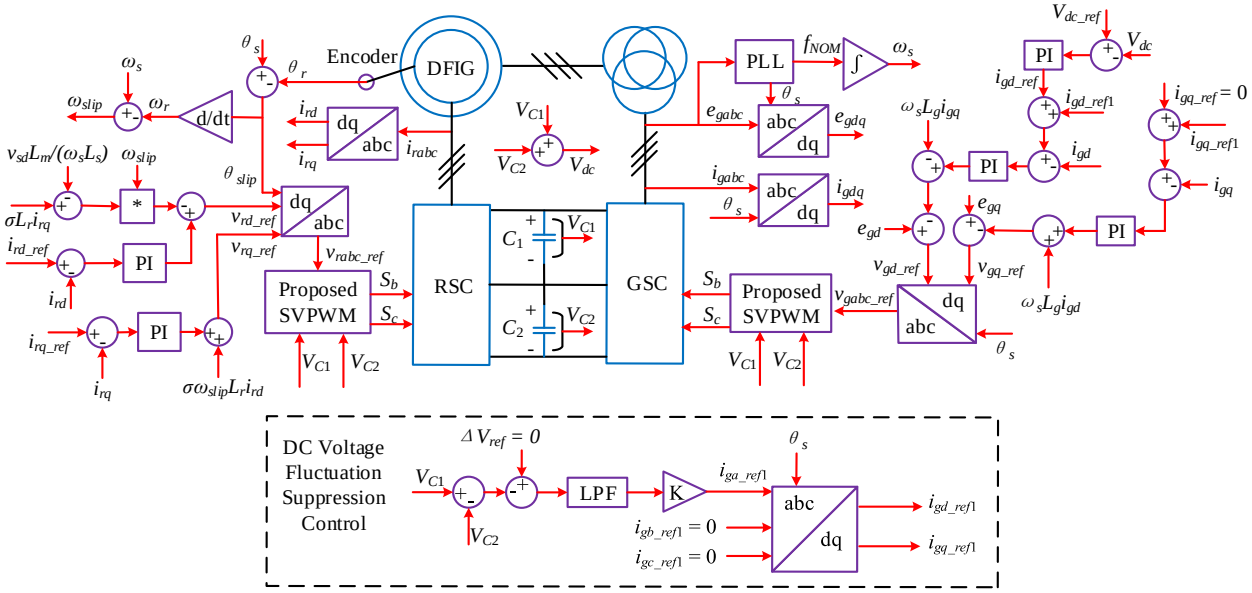


Figure 3. Control strategy for FSTP topology-based back-to-back converter in DFIG-WT

For the FSTP GSC, an outer voltage control loop is formed to keep the DC-bus voltage steady, in which case constant DC voltage supply to the RSC can be guaranteed. For the inner-loop current control, the coupling terms $-\omega_s L_g i_{gq}$ and $\omega_s L_g i_{gd}$ are eliminated, and the PI controllers for the d and q current components are designed to minimize the harmonic components so that sinusoidal three-phase current waveforms are maintained. In particular, a DC voltage fluctuation suppression control loop is utilized in the FSTP GSC to decrease the difference between V_{C1} and V_{C2}. In the proposed control strategy, the instantaneous dc current component produced in phase A (the faulty phase) is fed back to the inner current control loop, and a proportional controller is applied. A LPF is used to remove the high-frequency components in the current.

4.3.4. Monitoring Aspects

After the power converter circuit in RSCAD is compiled and run in DRTS, the control algorithms in Simulink are uploaded to CHIL and performed to make the FSTP GSC and RSC operate normally. The plots of the key measurements are added to the “Runtime” interface in RSCAD. For example, the DC-bus voltage should be maintained at a nearly constant value. By refreshing the plots in RSCAD or monitoring the signal in Simulink by using a scope, the variations in DC-bus voltage can be clearly observed. Since the simulation is in real time, the tracking performance of the signal will vary instantly with the modifications in the parameters of controllers. When the circuit parameters are changed in RSCAD, the power converter circuit needs to be complied again to update the changes. For the other measurements, the monitoring processes are the same.

4.4 Data Management and Processing

The values to be used as the inputs to CHIL are the three-phase grid voltages V_{gabc}, three-phase grid currents I_{gabc}, three-phase rotor currents I_{rabc}, the grid synchronous angular frequency ω_s, the rotor electrical angular speed ω_r, and the DC-link capacitor voltages V_{C1} and V_{C2}. All of the aforementioned values are measured in SI units. The converter circuit parameters are given in Table 1.

Table 1. Converter circuit parameters

Variables	Value	Units
Grid-Side Resistance R_g	0.00567	Ω
Grid-Side Inductance L_g	0.567	H
Rotor Resistance R_r	0.003	Ω
Rotor Inductance (including the leakage and mutual parts) L_r	0.578	H
DC-link Capacitance C_1, C_2	10000	μF

5 Results and Conclusions

5.1 Simulation Results in Matlab/Simulink2016a

To verify the reliability of the proposed FSTP GSC and RSC in DFIG-WT, simulation studies are conducted in Matlab/Simulink2016a. A 1.5MW DFIG wind energy generation system is chosen, and the system parameters are illustrated in Table 2.

Table 2. Parameters of DFIG-WT in Matlab/Simulink2016a

Parameter	Value	Unit
Rated Power S_g	1.5	MVA
Rated Frequency F_{nom}	50	Hz
Rated Stator Voltage	575	V
Stator Resistance R_s	0.023	p.u.
Rotor Resistance R_r	0.016	p.u.
Stator Inductance L_{ls}	0.18	p.u.
Rotor Inductance L_{lr}	0.16	p.u.
Magnetizing Inductance L_m	2.9	p.u.
Friction Factor F	0.01	p.u.
Inertia Constant H	0.685	s
Pairs of Poles p	3	\
DC Bus Capacitor C	10000	μF
Rated Wind Speed v_w	11	m/s

The simulation results for FSTP back-to-back converter based DFIG-WT with wind speed fluctuation and short-term grid voltage drop are displayed in Figure 4.

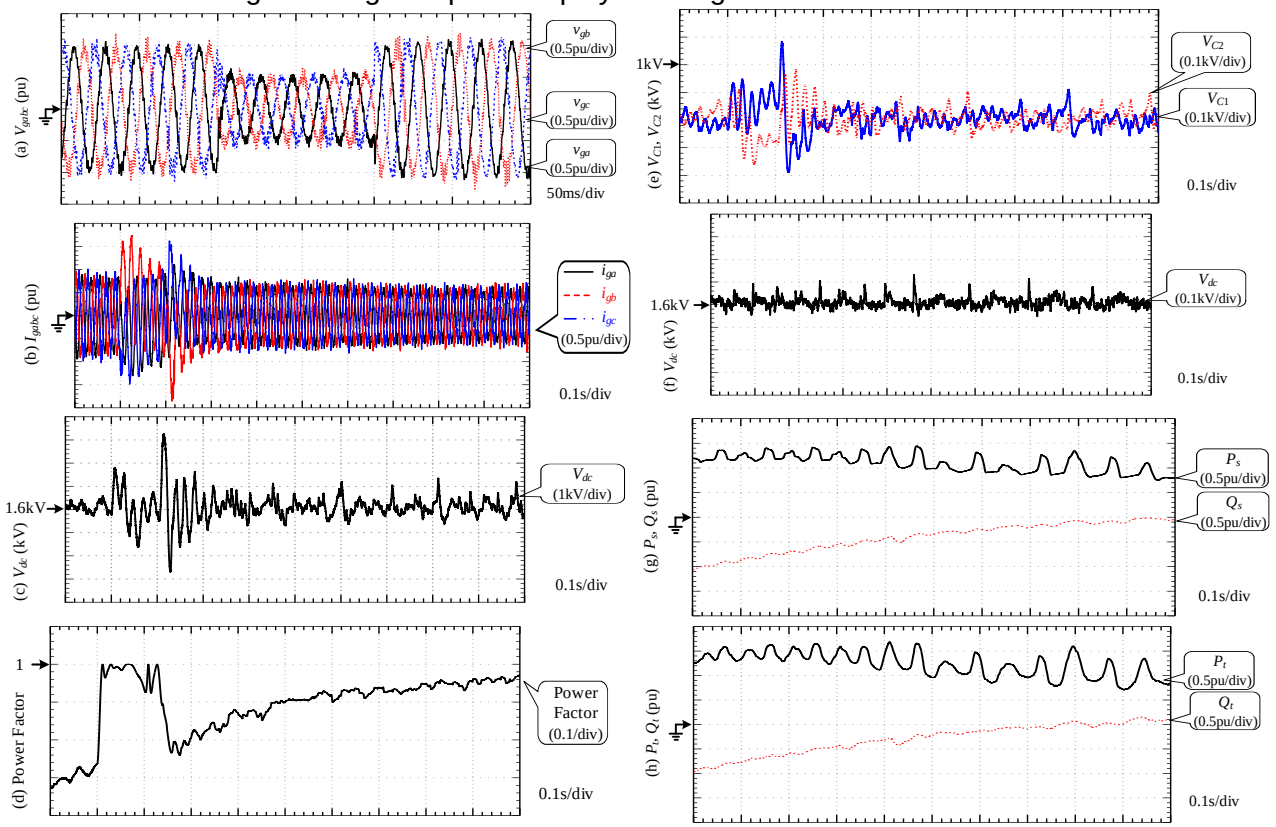


Figure 4. Simulation results for the FSTP back-to-back converter in a 1.5MW DFIG-WT (a) three-phase grid voltages V_{gabc} (pu); (b) three-phase grid currents I_{gabc} (pu); (c) DC-bus voltage V_{dc} (kV) with GSC reconfigura-

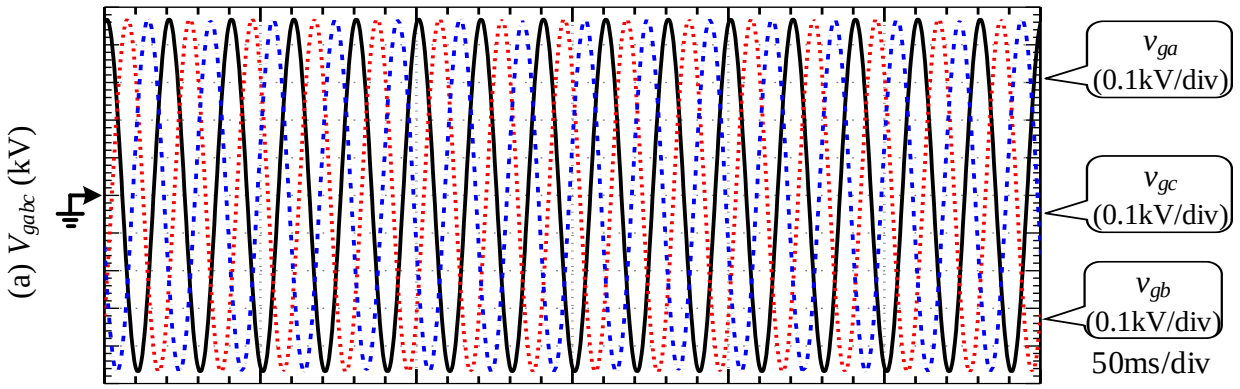
tion; (d) output power factor (e) Upper and lower DC-link capacitor voltages V_{C1} and V_{C2} (kV); (f) DC-bus voltage V_{dc} (kV) with RSC reconfiguration; (g) Stator active power P_s (pu) and reactive power Q_s (pu); (h) Total output active power P_t (pu) and reactive power Q_t (pu)

As can be seen from the Figure 4(a), during 0.1s to 0.2s, the amplitudes of three-phase grid voltages drop to 0.5p.u. From Figure 4(b), the effects of the short-term grid voltage sag on phase A grid current can hardly be observed as there is no controllable power switches in the DC-bus. From Figure 4(c) it can be seen that almost constant voltage supply for the RSC can still be ensured after the voltage sag period. In addition, unity power factor can be achieved after GSC reconfiguration, which is displayed in Figure 4(d). Besides, the DC-link capacitor voltage balancing is achieved by the proposed voltage suppression control strategy, as is shown in Figure 4(e).

In the case that RSC is reconfigured into FSTP topology, wind speed step change from 15m/s to 8m/s at t = 0.1s is considered. Similarly, the value of DC-bus voltage has to increase, but much less influence is observed compared to the former situation for GSC reconfiguration, as is displayed in Figure 4(f). From Figures 4(g) and (h), acceptable regulation for the stator and total power flows can be ensured. With the acceptable power quality and sufficient real power delivered to the grid in the post-fault operation of DFIG-WT, disconnection form the grid is avoided and continuous operation for power supply to the grid can be achieved.

5.2 Results Derived in CHIL Setup

The experimental results for the operation of FSTP GSC are illustrated in Figures 5 and 6. Since the GSC is directly connected to the grid and no distortions are injected, the three-phase grid voltages are in perfect sinusoidal waveforms as displayed in Figure 5(a). The three-phase grid current waveforms are shown in Figure 5(b), and current unbalance and phase shifts can be observed, which are caused by the modeling of a phase connected to the common point in DRTS. In Figure 6(a), a step change of DC-bus voltage from 1.4kV to 1.6kV is presented, demonstrating the performance of the control loop in GSC for the actual DC-bus voltage value to track the change in the reference value within 2 seconds. Besides, the controller performance in balancing the upper and lower DC-link capacitor voltages is validated in Figure 6(b), and the maximum difference between these two voltages is around 20V, which is about 1.25% of the DC-bus voltage value. Therefore, the influence of DC-link capacitor voltage unbalance on DC-bus voltage utilization rate can nearly be neglected, which fully demonstrates the validity of the proposed control algorithm in FSTP GSC.



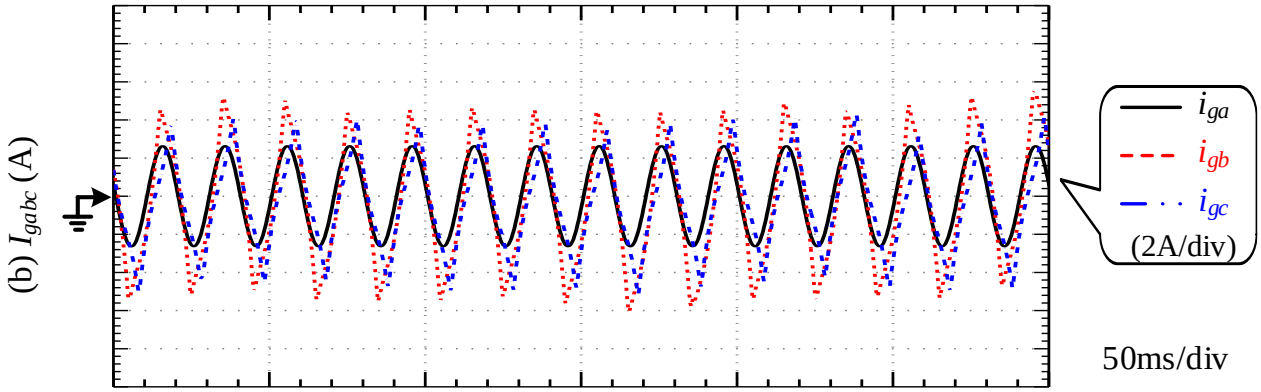


Figure 5. Experimental results for FSTP GSC (a) three-phase grid voltages V_{g_abc} (kV) and (b) three-phase grid currents I_{g_abc} (kA)

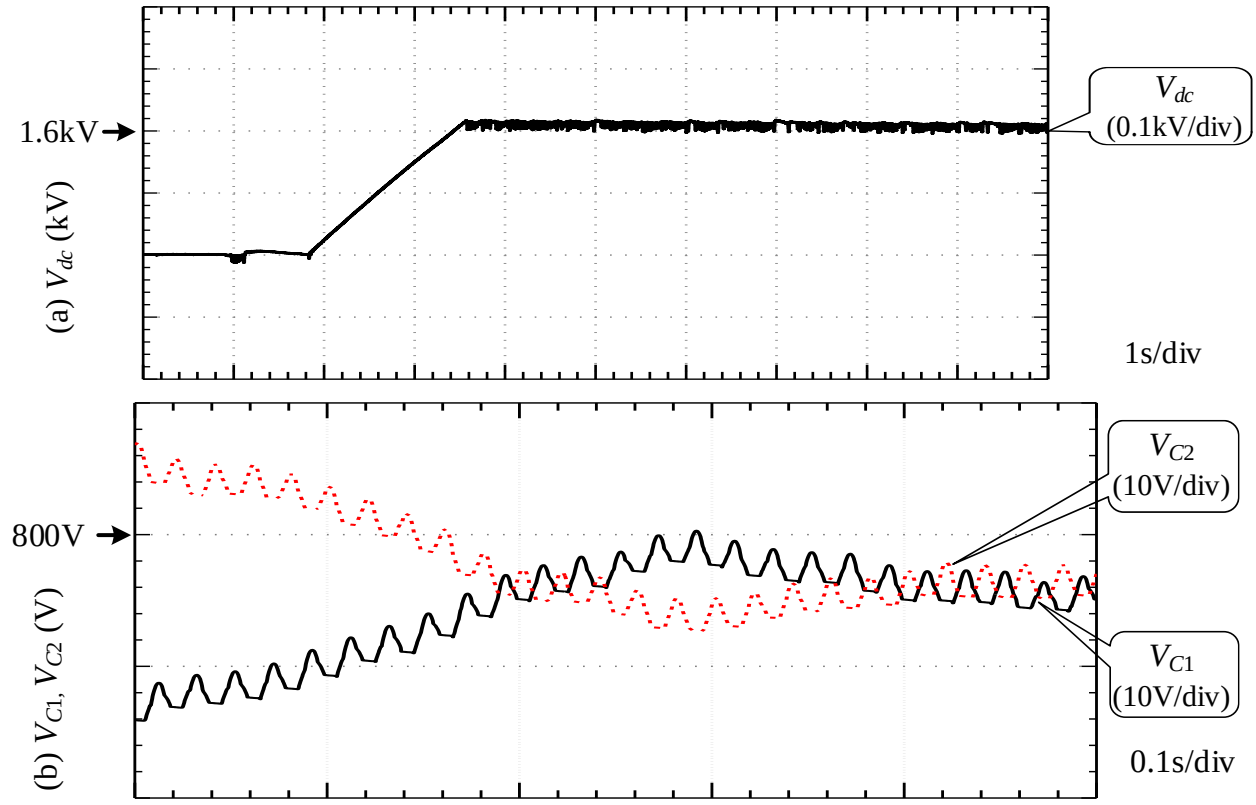


Figure 6. Experimental results for FSTP GSC (a) DC-bus voltage V_{dc} (kV) with step change from 1.4kV to 1.6kV and (b) DC-link capacitor voltages V_{C1}, V_{C2} (V)

When an open-circuit fault occurs in one of the bridge arms in RSC, the performance of the PI current controllers in the rotor-side control system is investigated, and the experiment results are displayed in Figures 7 - 10.

A step change of the *d*-axis rotor current reference value i_{rd_ref} from 0 to 0.8A is presented in Figure 7, and it is observed from Figure 7(a) that the actual *d*-axis rotor current i_{rd} tracks the reference value within a short time period (approximately 0.01s), and the rotor active power P_r also tracks the change instantly as is illustrated in Figure 8(a). Spikes in Figures 7(b) and 8(b) at the moment of i_{rd} step change are induced by the time delays during the signal exchange process between DRTS and the controller.

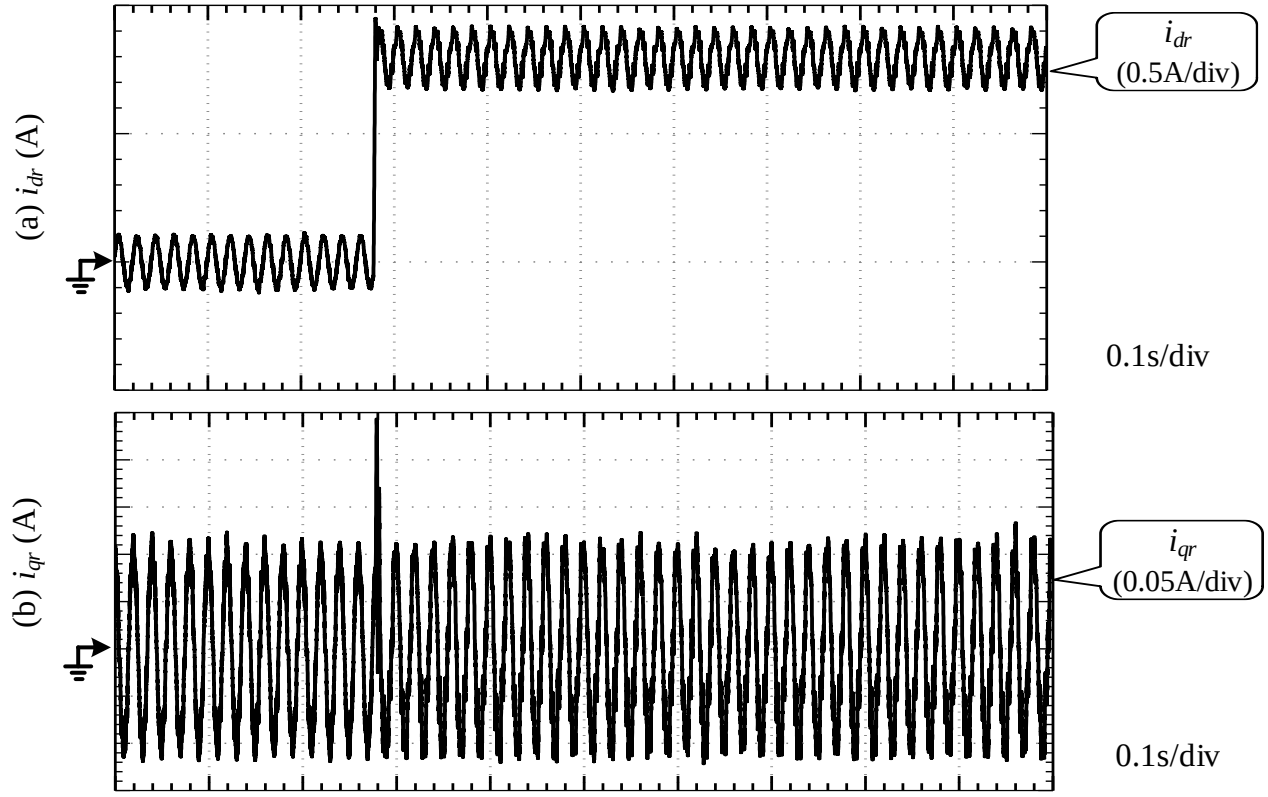


Figure 7. Experimental results for (a) i_{rd} (A) and (b) i_{rq} (A) with the step change of i_{rd_ref} from 0 to 0.8A

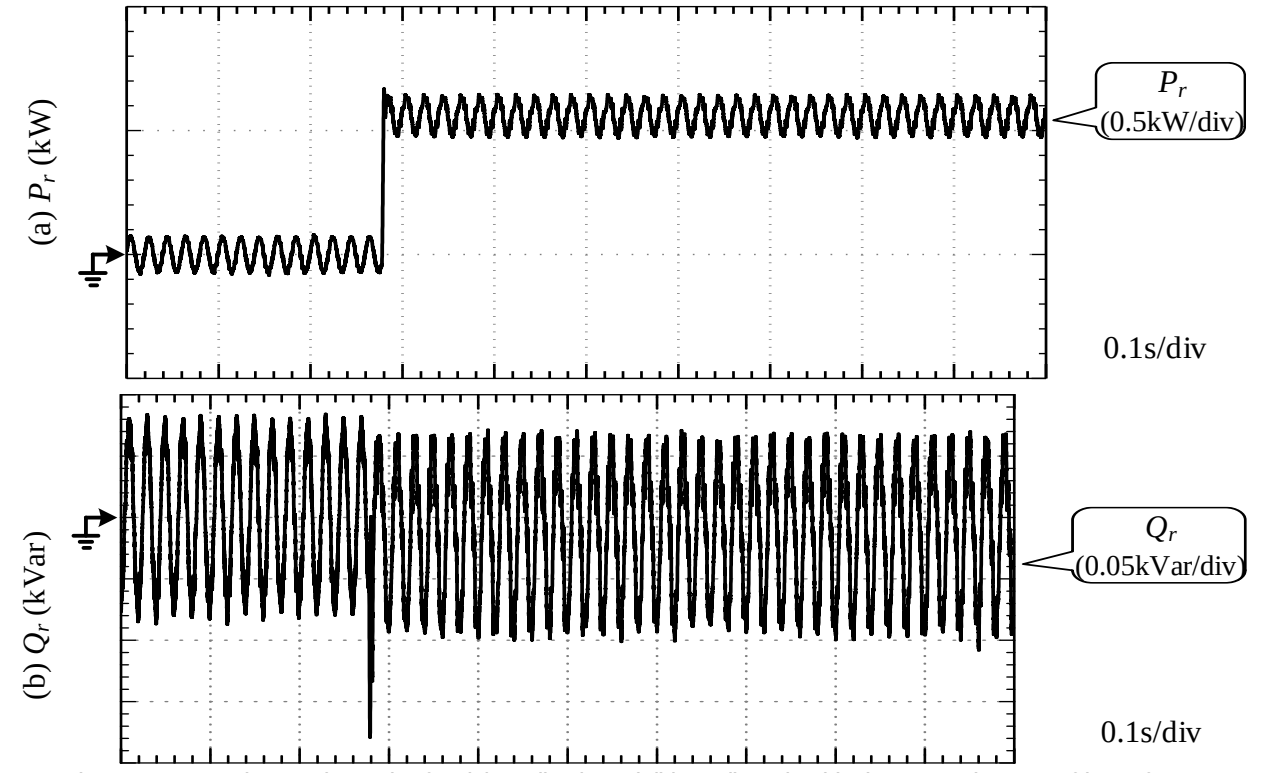


Figure 8. Experimental results for (a) P_r (kW) and (b) Q_r (kVar) with the step change of i_{rd_ref} from 0 to 0.8A

In Figures 9 and 10, there is a step change of the *q*-axis rotor current reference value i_{rq_ref} from 0 to 2A. Similarly, the actual *q*-axis rotor current i_{rq} tracks the reference change quickly (approximately 0.01s), and the rotor reactive power Q_r also changes from 0kVar to around -1.4kVar swiftly as is depicted in Fig. 10(b). In addition, spikes in the *d*-axis rotor current i_{rd} and the rotor active power P_r

are observed due to time delays caused in the experimental implementation process.

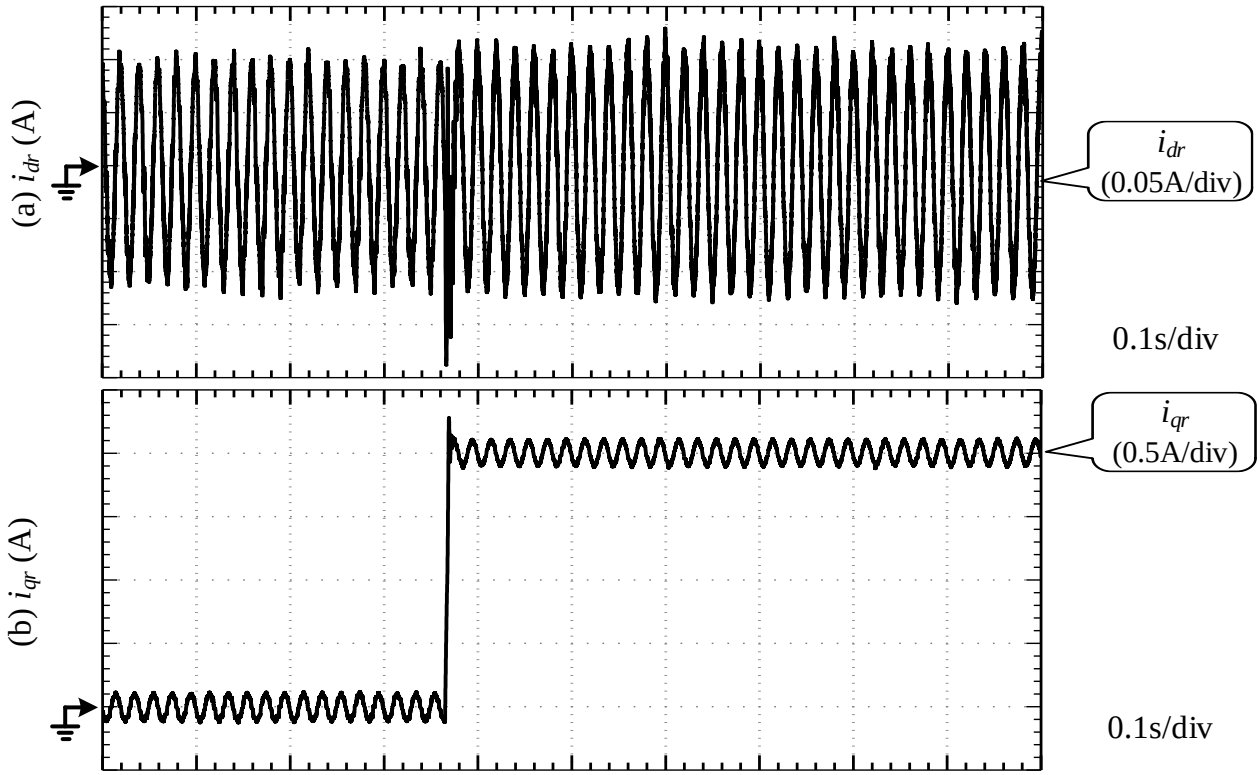


Figure 9. Experimental results for (a) i_{rd} (A) and (b) i_{rq} (A) with the step change of i_{rq_ref} from 0 to 2A

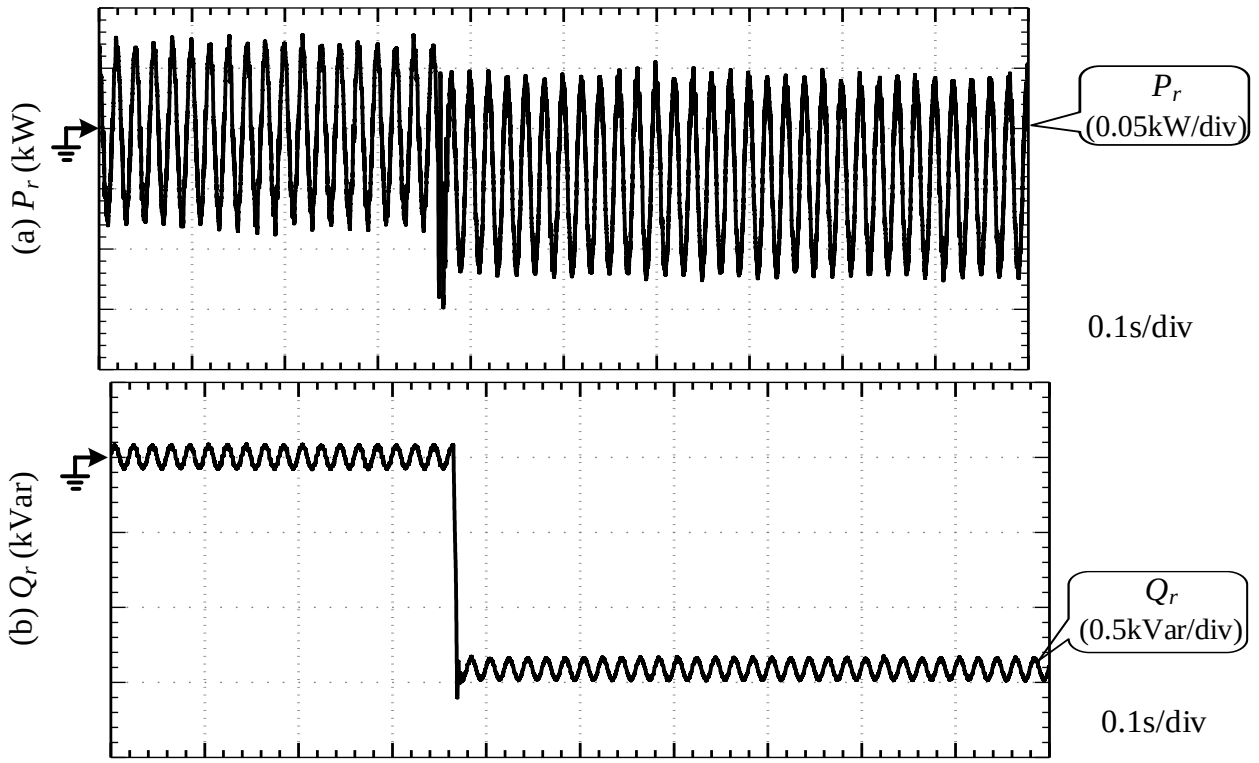


Figure 10. Experimental results for (a) P_r (kW) and (b) Q_r (kVar) with the step change of i_{rq_ref} from 0 to 2A

5.3 Conclusions

According to the results, the following conclusions can be derived:

The performance of the FSTP back-to-back converter in DFIG-WT is verified by simulation results in Matlab/Simulink:
(1) Nearly sinusoidal three-phase grid current waveforms are maintained shortly after the grid voltage sag is removed, which demonstrates the effectivity of the proposed modulation technique.
(2) There is no significant increase in the DC-bus voltage value after FSTP topology is used to replace the SSTP one, and the fluctuation in the DC-bus voltage is acceptable and it does not deteriorate the performance of RSC too much.
(3) Unity power factor can be achieved by using the proposed FSTP topology.
(4) The difference between V_{C1} and V_{C2} is maintained within a relatively small range and good voltage balancing effect is achieved.
(5) The reasonable control of stator active and reactive power ensures the continuous operation of DFIG-WT with FSTP RSC.
To further demonstrate the validity of the proposed control algorithms, small time-step simulations of FSTP GSC and RSC are conducted in DRTS, with the control algorithms performed in CHIL:
(1) More realistic situations are applied, and time delays and noises introduced during the implementation can lead to distortions in the waveforms derived in DRTS.
(2) For FSTP GSC: The tracking performance of the grid-side voltage controller is demonstrated to be excellent, and few fluctuations in V_{dc} are observed. Good DC-link voltage balancing effect is obtained and the difference between V_{C1} and V_{C2} is within $\pm$20V.
(3) For FSTP RSC: The actual *d*-axis and *q*-axis rotor currents track the changes in respective rotor current reference values in 0.01s, and the rotor active and reactive power vary accordingly and swiftly, which demonstrates the excellent current controller performance in FSTP RSC.

6 Open Issues and Suggestions for Improvements

6.1. Open Issues
(1) The scenario with open-circuit faults simultaneously in GSC and RSC has not been investigated.
(2) In the experiment the DFIG model is not included.

6.2. Suggestions for Improvements
(1) The waveforms of three-phase grid currents are not sinusoidal enough, and further improvement in the control strategy is required.
(2) The fluctuations in the rotor active and reactive power should be mitigated in forthcoming researches.
(3) Wear down of the DC-link capacitors can be taken into consideration for more practical cases.

7 Dissemination Planning

1 journal article and 1 conference paper will be published based on the results in this project, and further publication may be possible as both sides agree to cooperate in the future.
The experimental results will be added to our papers as important parts. We will take part in an IEEE conference to introduce our project and indicate the importance of it, and ask for advice from other researchers in similar research fields. Apart from that, we are going to invite them to deliver our ideas to their research institutions. After that, the paper will be published in IEEE journals to distribute our results to more researchers and students. Our results will be illustrated in posters and it will be displayed in our university, and we will arrange visit and meetings to other universities and research institutions in the UK and in other countries to deliver our results by giving presentations and displaying our posters. In addition, the results of this proposed research will be involved in the training process for the undergraduate and MSC projects in University of Liverpool (UoL). These students will do their research based on the results of this work and they may further develop some new ideas to the existing results, which may help us improve the original method and produce a better prototype of the product. After the undergraduate and postgraduate students graduate from UoL, they will take these ideas into further education or work, and distribute the ideas to their colleagues, which leads to more discussion on this topic and create more ideas. We will keep contact with these students and frequently communicate with them to discuss on this topic. Furthermore, we will collaborate with the researchers who are interested in this area, and we are going to continue working on this topic to develop more outcomes, and we will contact corresponding enterprises to apply our products in practical applications.

8 References

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9 Annex

9.1 List of Figures

9.2 List of Tables

9.3 Annex 1

Nomenclature

V, I, ϕ	Constant Values of Voltage, Current and Flux
v, i, φ	Instant values of voltage, current and flux
V_{dc}, V_{ref}	DC-link voltage and reference voltage value
v_{AN}, v_{BN}, v_{CN}	Instant values of three-phase voltages at points A, B and C with respect to the neutral point N
V_m	Amplitudes of the three-phase voltages
e	Instant values of voltage supply
V_{C1}, V_{C2}	Instant values of voltages on DC-link capacitors C_1 and C_2
i_{C1}, i_{C2}	Instant values of currents through DC-link capacitors C_1 and C_2
R_g, R_s, R_r	Resistances on the grid, stator and rotor
L_m, L_{ls}, L_{lr}	Mutual inductance, stator leakage inductance and rotor leakage inductance
L_g, L_s, L_r	Inductances on the grid, stator and rotor ($L_s = L_m + L_{ls}$; $L_r = L_m + L_{lr}$)
σ	Leakage flux factor: $\sigma = 1 - [L_m L_m/(L_r L_s)]$
P, P_s, P_r	Total output active power, stator active power, and rotor active power
Q, Q_s, Q_r	Total output reactive power, stator reactive power, and rotor reactive power
d_{00}, d_{10}, d_{11}, d_{01}	Duty ratios of active time for voltage vectors V_{00}, V_{10}, V_{11}, V_{01}
d_b, d_c	Duty ratios of active time for the switching functions S_b and S_c
f_{NOM}	Nominal grid frequency
θ_s, θ_r	Grid voltage angle and rotor angle
ω_s, ω_{slip}, ω_r, ω_m	Nominal grid angular frequency, slip angular frequency, electrical rotor angular speed and mechanical rotor angular speed
T_s, T_{sw}	Sampling time and switching time
T_e, T_m	Electromagnetic torque, mechanical/shaft torque
n_p	Number of pole pairs
J	Inertia of wind turbine
Subscripts	
s, r	Stator and rotor
a, b, c	Phase A, B, C
A, B, C	Point A, B, C

α, β	Stationary reference frame
d, q	Synchronous reference frame
$\_ref$	Reference value
$\_ref1$	Transient DC reference value