



P-HIL Tutorial

key design factors

Oct 2019

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EGSTON POWER ELECTRONICS PRODUCT PORTFOLIO

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Power Amplifiers

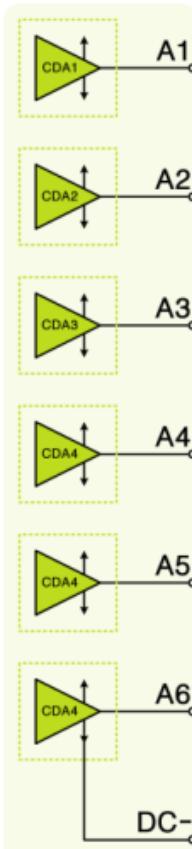
CSU 100 Systems: 100 kVA



CSU 200 Systems
• 200 kVA
• Up to 1.2 MVA



1 System – Various Configurations

Configuration	Free amplifiers	Three-phase + N	Three-phase	1xAC single phase 1x DC-bipolar	DC-unipolar
	A1 A2 A3 A4 A5 A6 DC-	A1 A2 A3 A4 A5 A6 DC-	L1 L2 L3 N	DC1 AC1 DC2 AC2 DC3 AC3	DC1 AC1 DC2 AC2 DC+ DC-

HIL Partner

High Speed Fibre Optic Interface
implemented

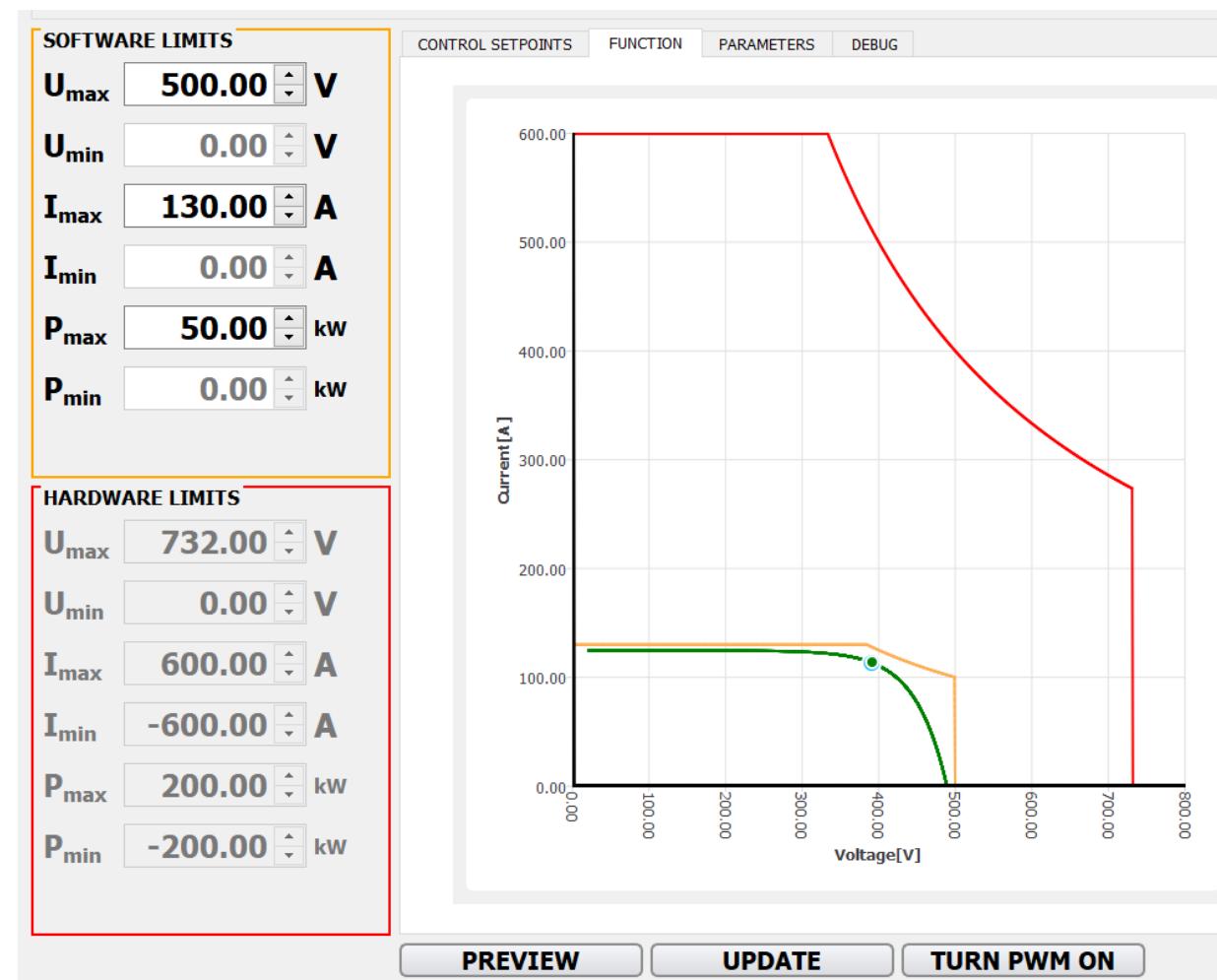


Interface in preparation



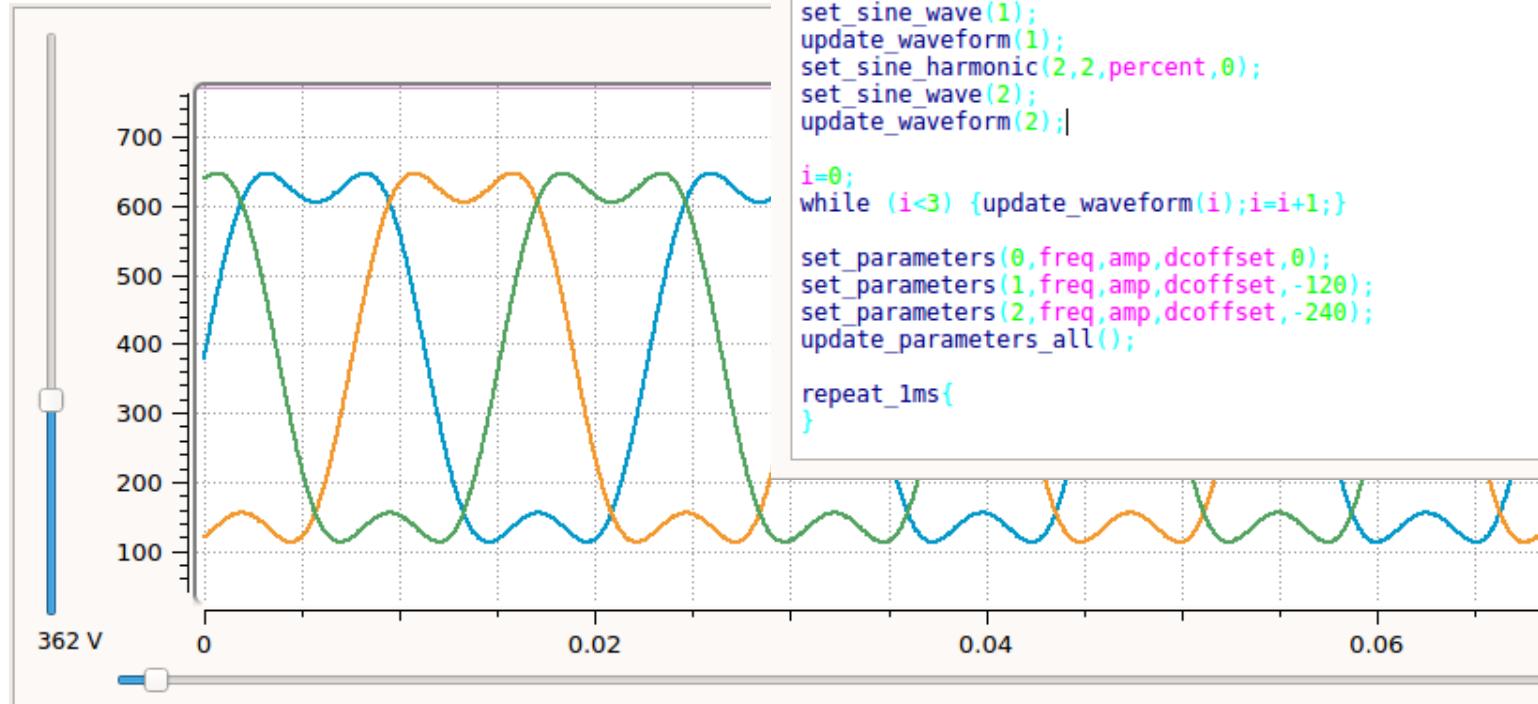
App: DC - Source

- 1 to 4 Quadrants
- Soft-Limits
- Multiple Curves
- Emulations
 - PV Panels
 - Batteries



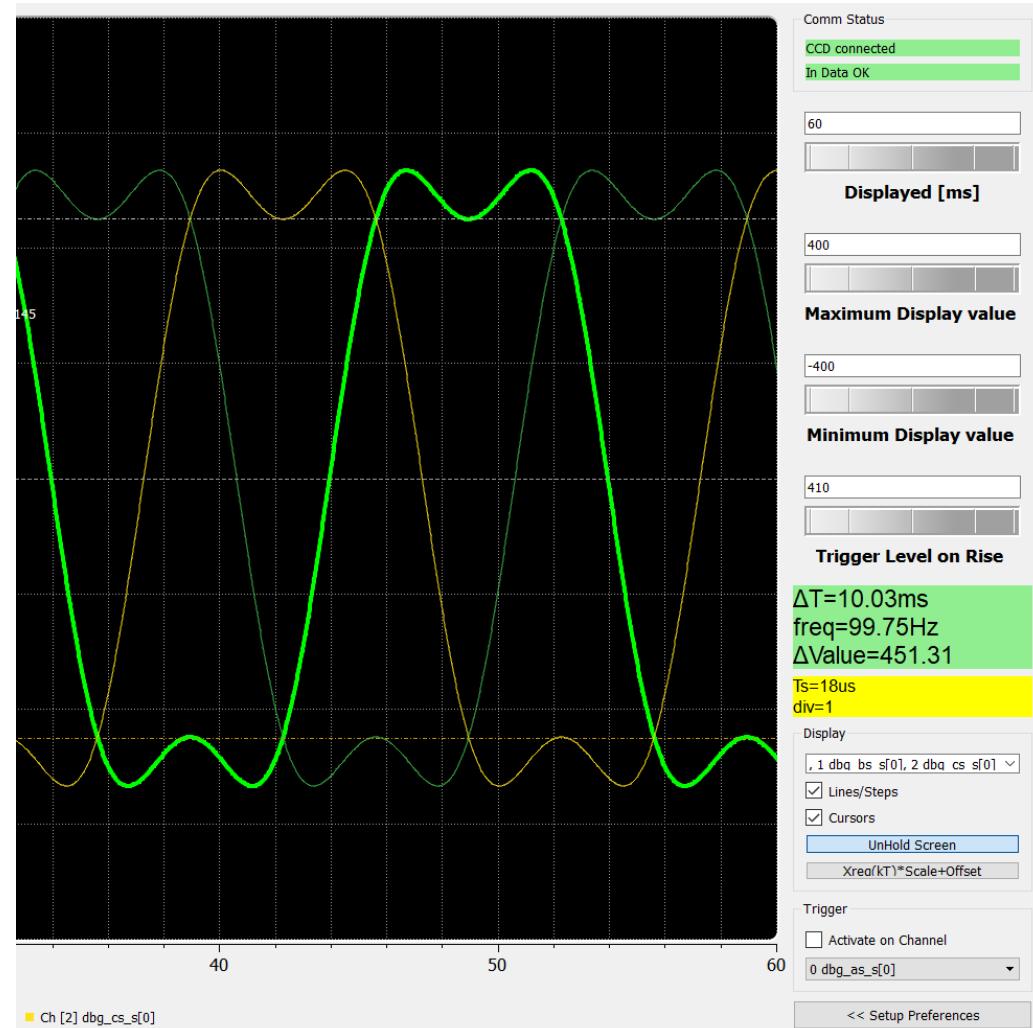
App: AC Source

- .. Script based editor
- .. Time base: Internal / External
- .. Trigger: Internal / External



App: Oscilloscope

- .: Online signal display
- .: Trigger
- .: Real-time data tracking
- .: Signal source
 - .: Real-time playback of recorded data streams

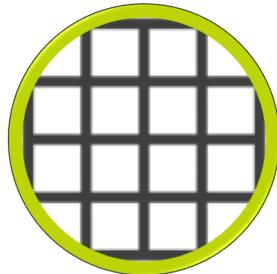




P-HIL TARGET MARKETS

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MARKETS & APPLICATIONS



SMART GRID

Applications

- Grid Emulator (50, 60, 400 Hz)
- Grid Load
- PV-Inverter Emulation
- Wind-Generator Emulation
- Impedance Spectroscopy
- UPS (Uninteruptible Power Supply) Emulation
- Grid Inverter Emulation
- Grid Motor / Generator Emulation



AUTOMOTIVE & TRANSPORT

Applications

Electrical drive train emulation

- Battery Emulator
- Drive Inverter Emulator
- Motor Emulator

eVehicle Applications

- eVehicle charging station emulator
- Test Bench for charging

Test Benches for combustion engine drive train

- Drive Inverter for electrical machines connected to combustion machines, wheel, gear boxes

Transportation

- Grid Emulator
- Machine Emulator
- Inverter Emulator
- Electrical drive train emulation



AEROSPACE & DEFENSE

Applications

- 400 Hz Supply Grid Emulator
- DC-Supply emulation
- 400 Hz Aerospace device emulator
- AC-DC Coupling Emulator
- Generator / Motor Emulator
- 400 Hz Inverter Emulator

OTHERS

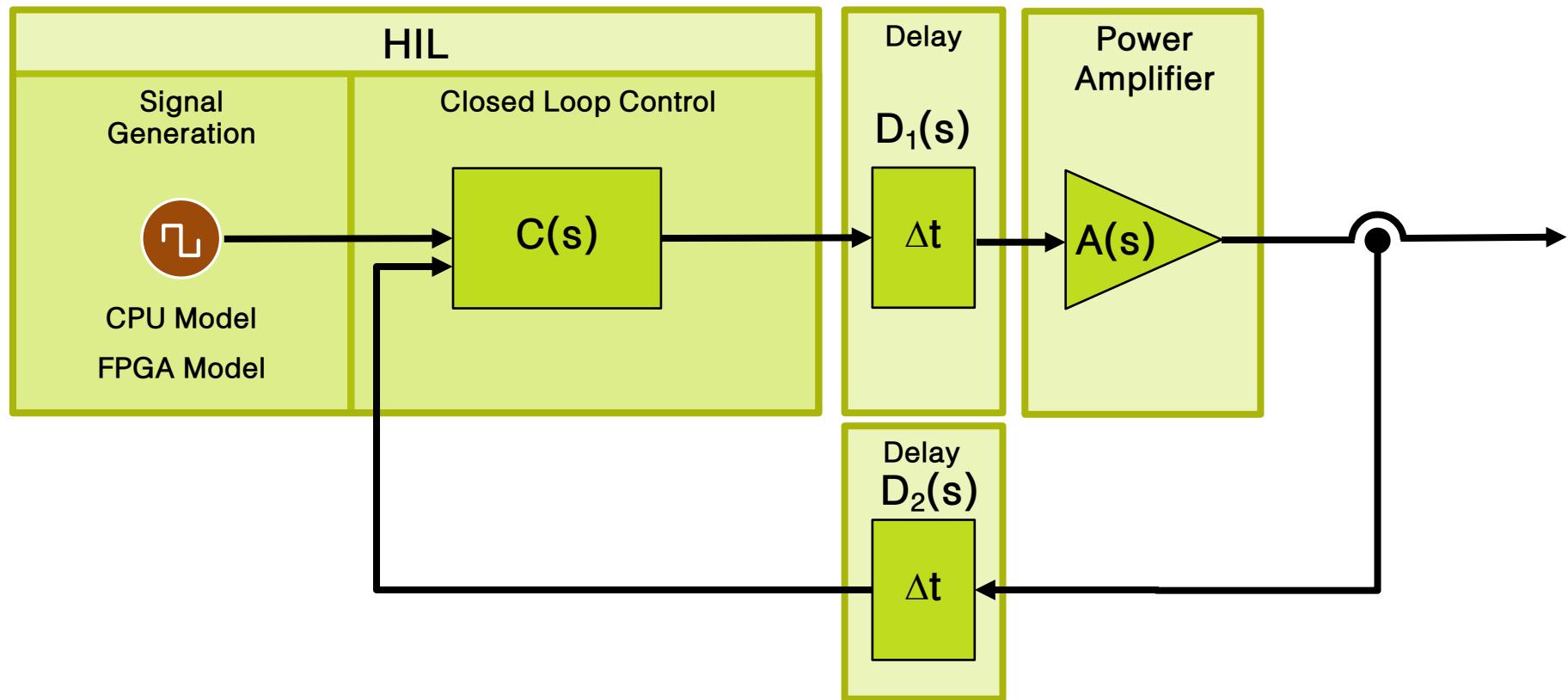
- Motor / Generator Emulator
- Motor Drive Inverter Emulator
- Motor Frequency Inverter Emulator



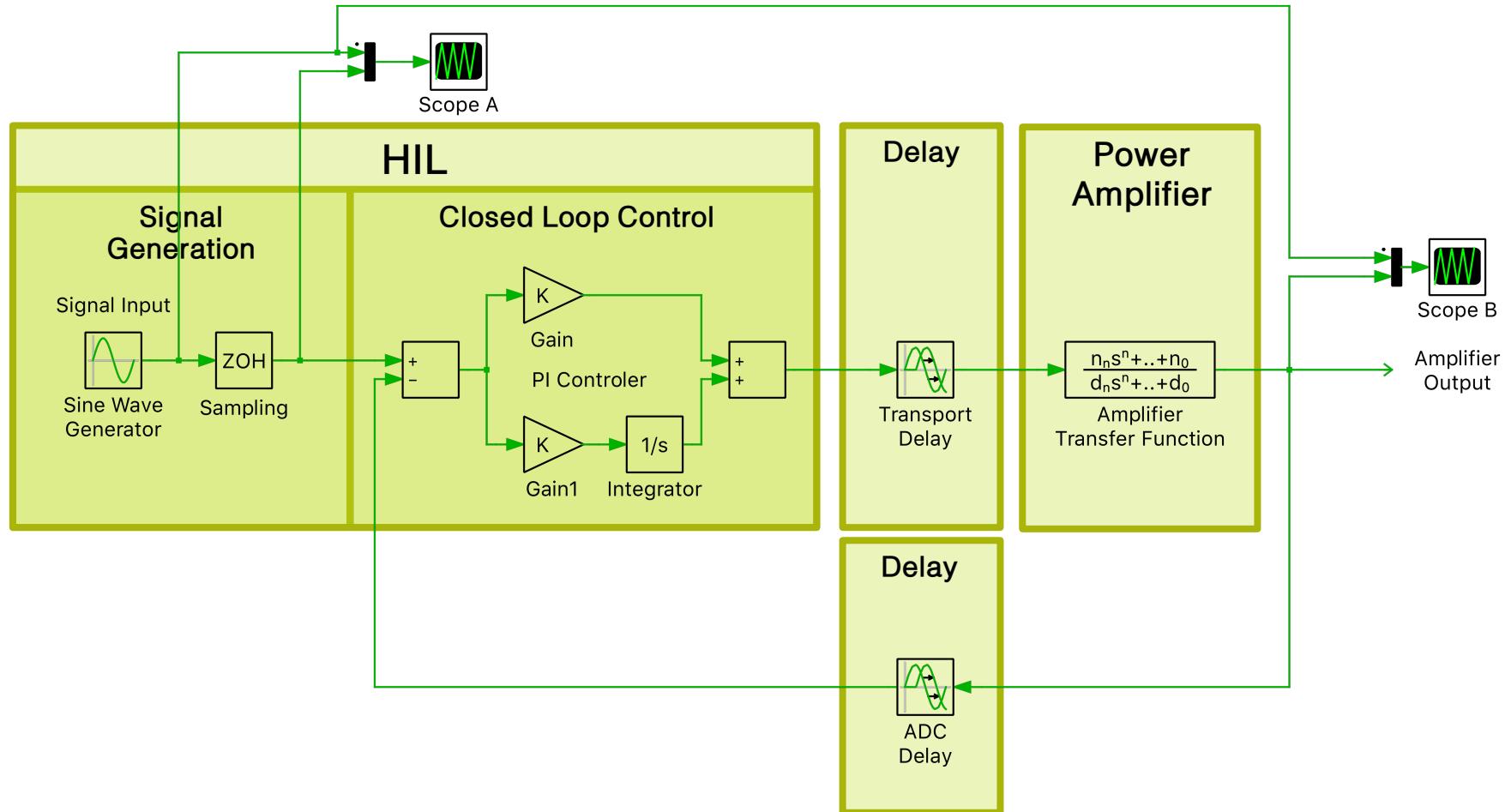
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Simplified P-HIL Model



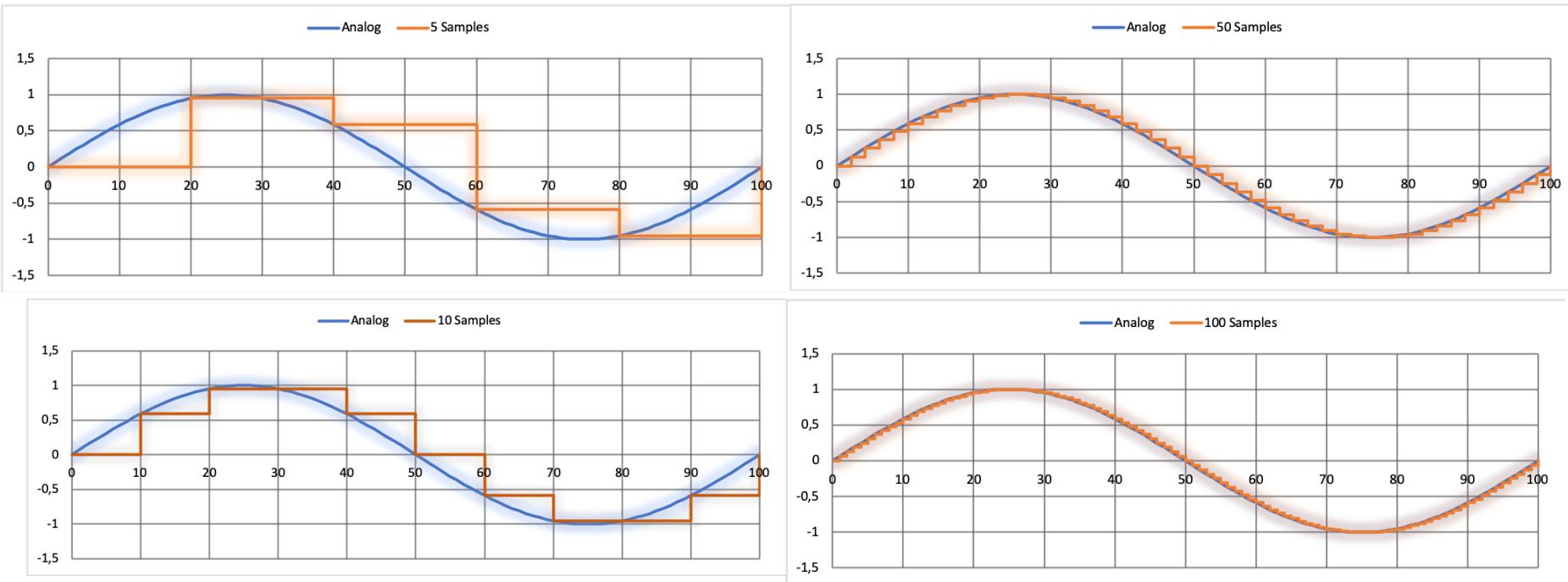
Simplified Simulation Model



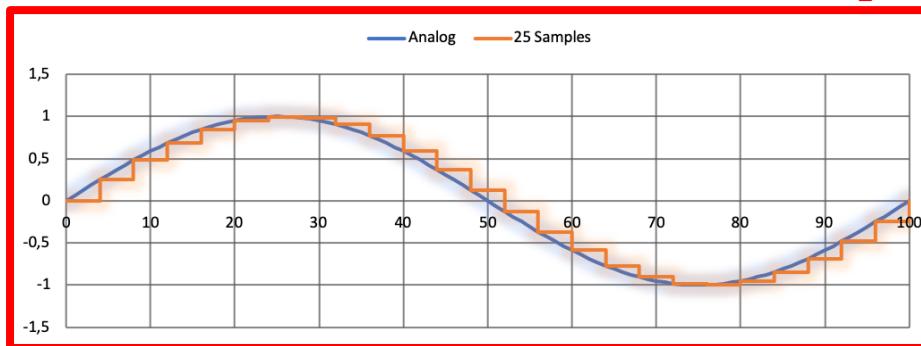
REQ 1: Model Bandwidth

- .. Definition: Model Bandwidth
 - .. What is the highest frequency (f_{Model_Max}) in the model that has to be controlled in a closed loop application in the P-HIL System
- .. **REQ 1: f_{Model_Max} : Maximum Model Frequency**
- .. Remarks:
 - .. It is not the fundamental frequency!
 - .. It can be
 - .. the highest harmonic you want to model
 - .. The highest „modulation“ frequency (eg impedance spectroscopy) you want to model

REQ 2: Signal Quality @ f_{Model_Max}



at least 25 set points per period @ f_{Model_Max}



REQ 2: Signal Quality @ f_{Model_Max}

- ..: Signal quality of generated signals
 - .: At f_{Model_Max} a curve shall be represented by at least 25 (better 50) samples for a full sine wave period

REQ 2: at least 25 set points per period @ f_{Model_Max}

REQ 3: Model Cycle Time

∴ Requirement Model Cycle Time:

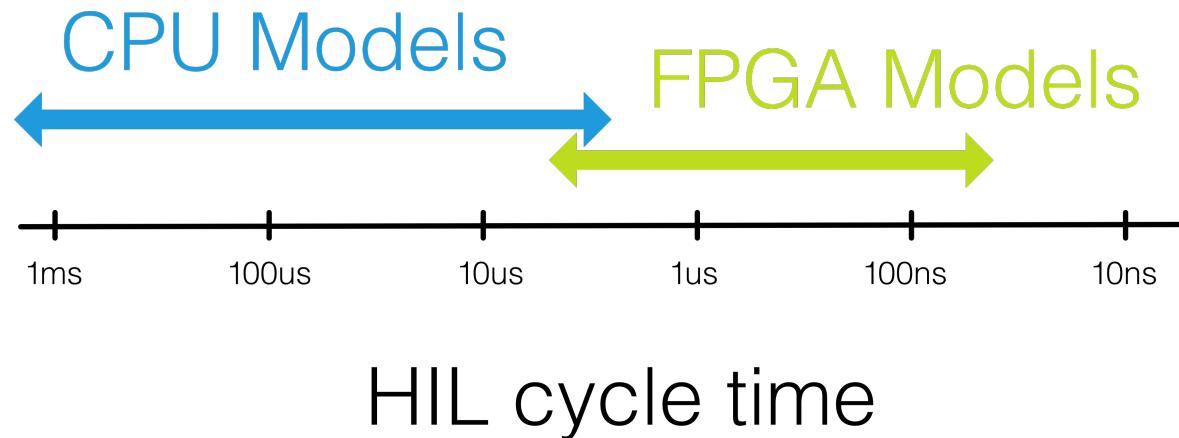
∴ REQ 3: $T_{Model_Cycle_Time} = \frac{1}{25 \cdot f_{Model_Max}}$

REQ 4: HIL CPU vs FPGA Technology

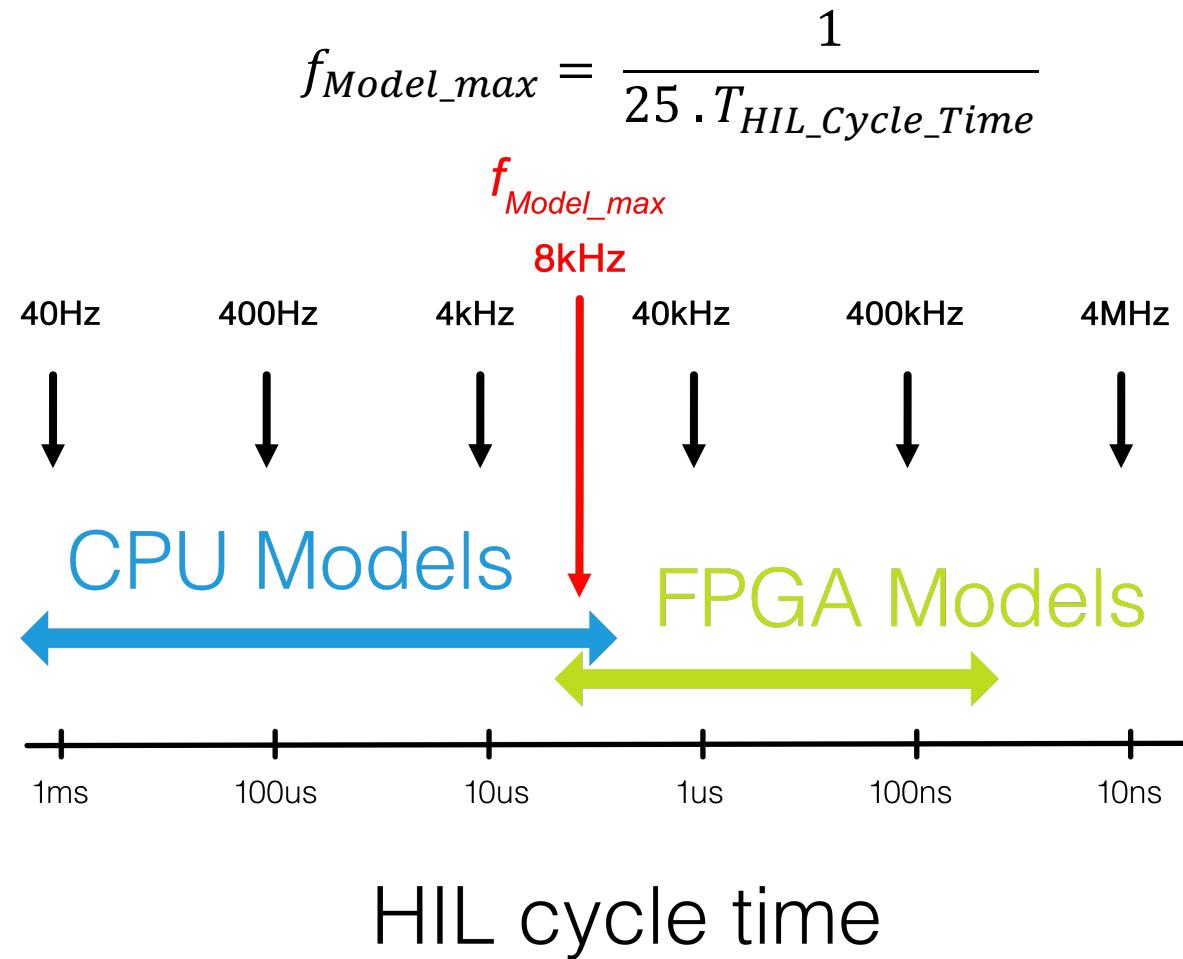
- .: Cycle time step size of the HIL real-time simulator: $T_{HIL_Cycle_Time}$

REQ 4: $T_{HIL_Cycle_Time} \leq T_{Model_Cycle_Time}$

- .: This REQ defines the required HIL rt-Processor technology



REQ 4: HIL CPU vs FPGA Technology

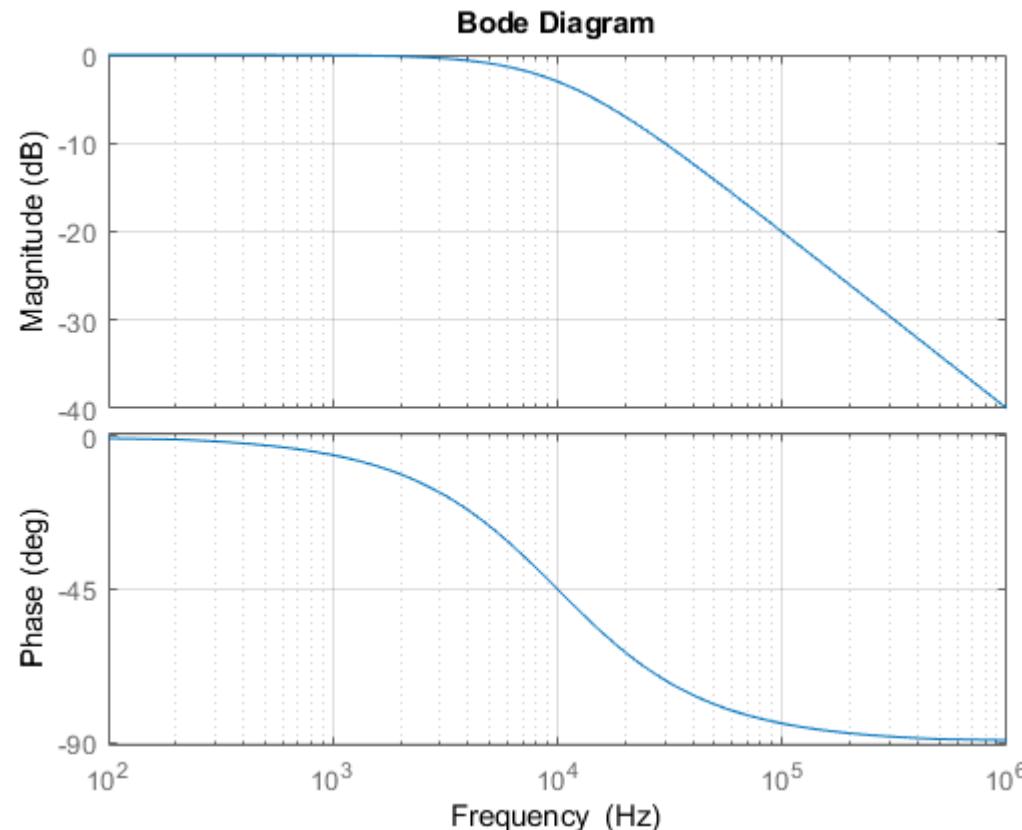


REQ 5: Power Amplifier Bandwidth

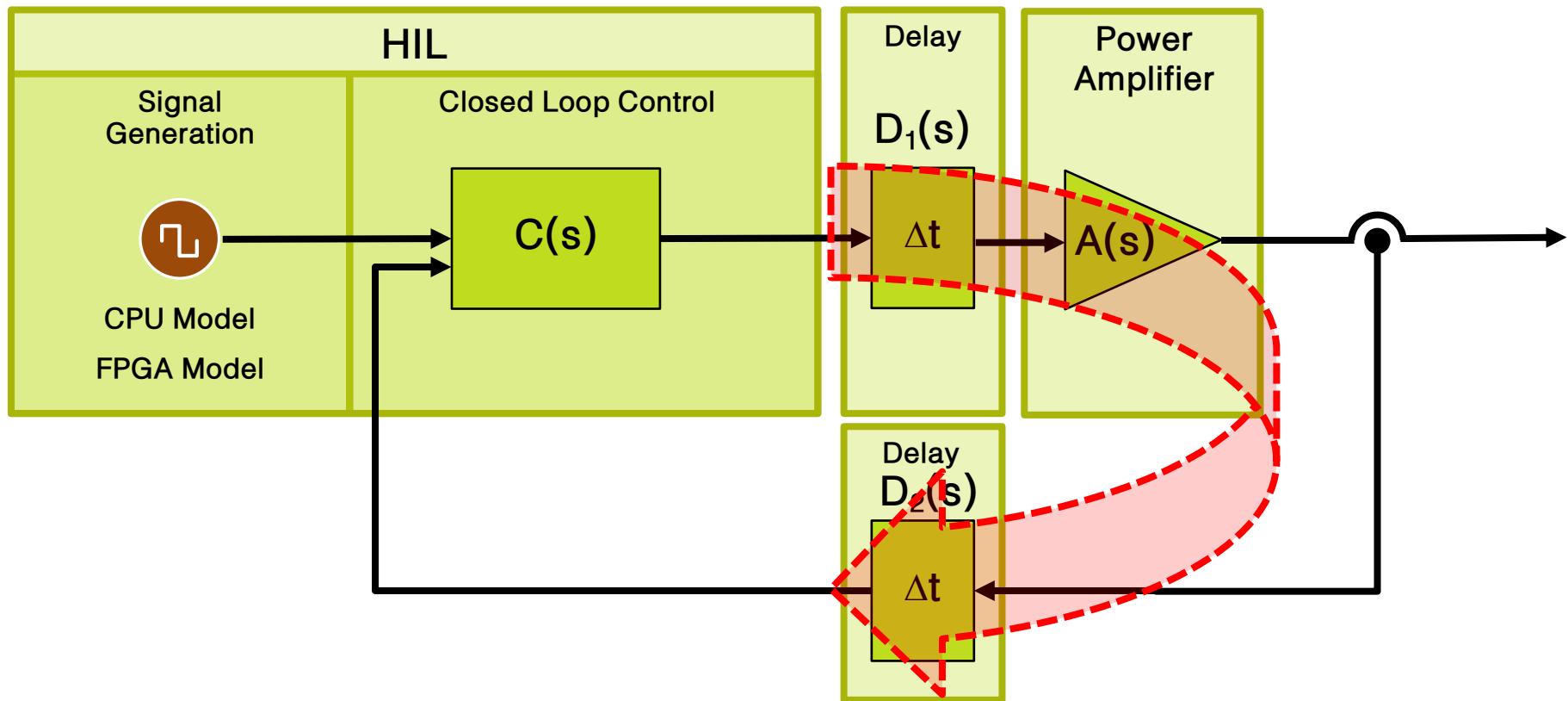
- .. At frequency: f_{Model_Max}
 - .. Amplifier Gain: < -1,5 dB
 - .. Amplifier Phase Shift: < -30°
- .. **REQ 5: Amplifier Bandwidth (-3dB)**
 - $f_{-3dB} > 1,5 \cdot f_{Model_Max}$
 - .. Amplifier Gain: -3 dB
 - .. Amplifier Phase Shift: < -45°

Amplifier Transfer Function

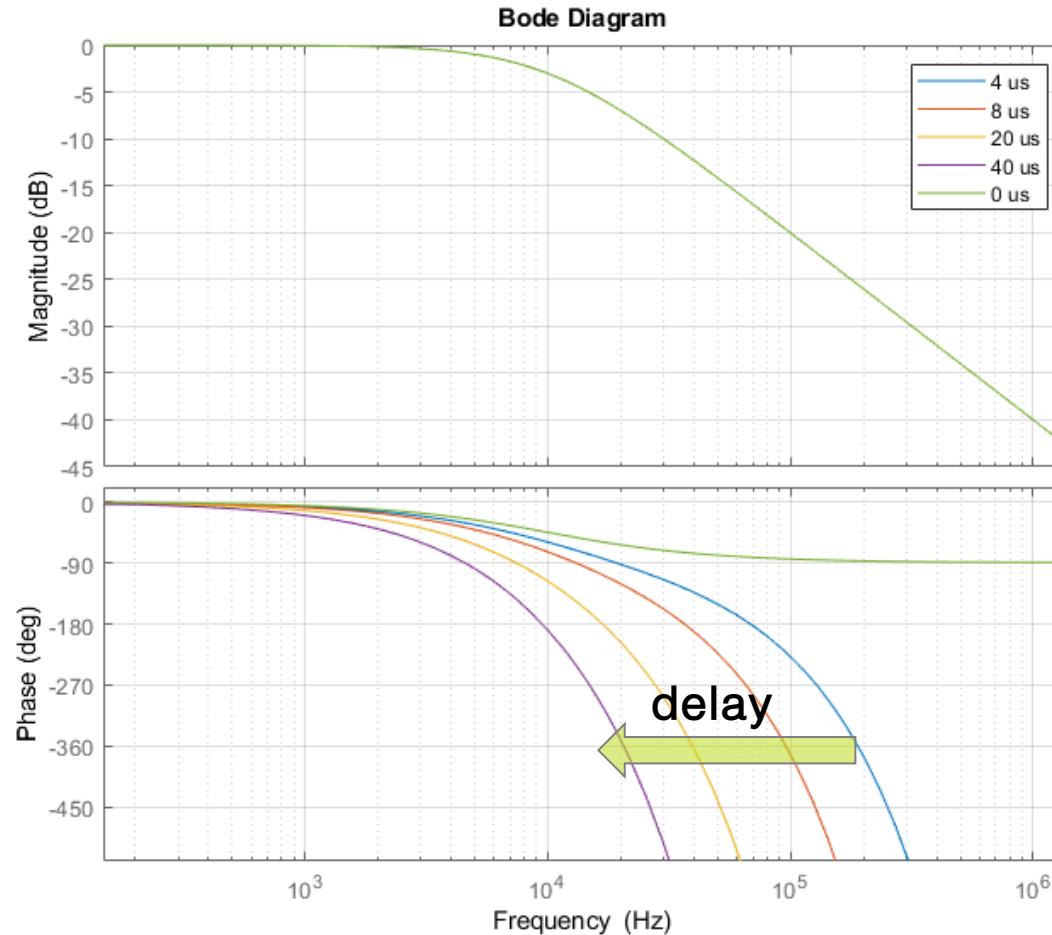
- .. Model requirement
 - .. For simple investigation:
1st order transfer function is sufficient to start investigation



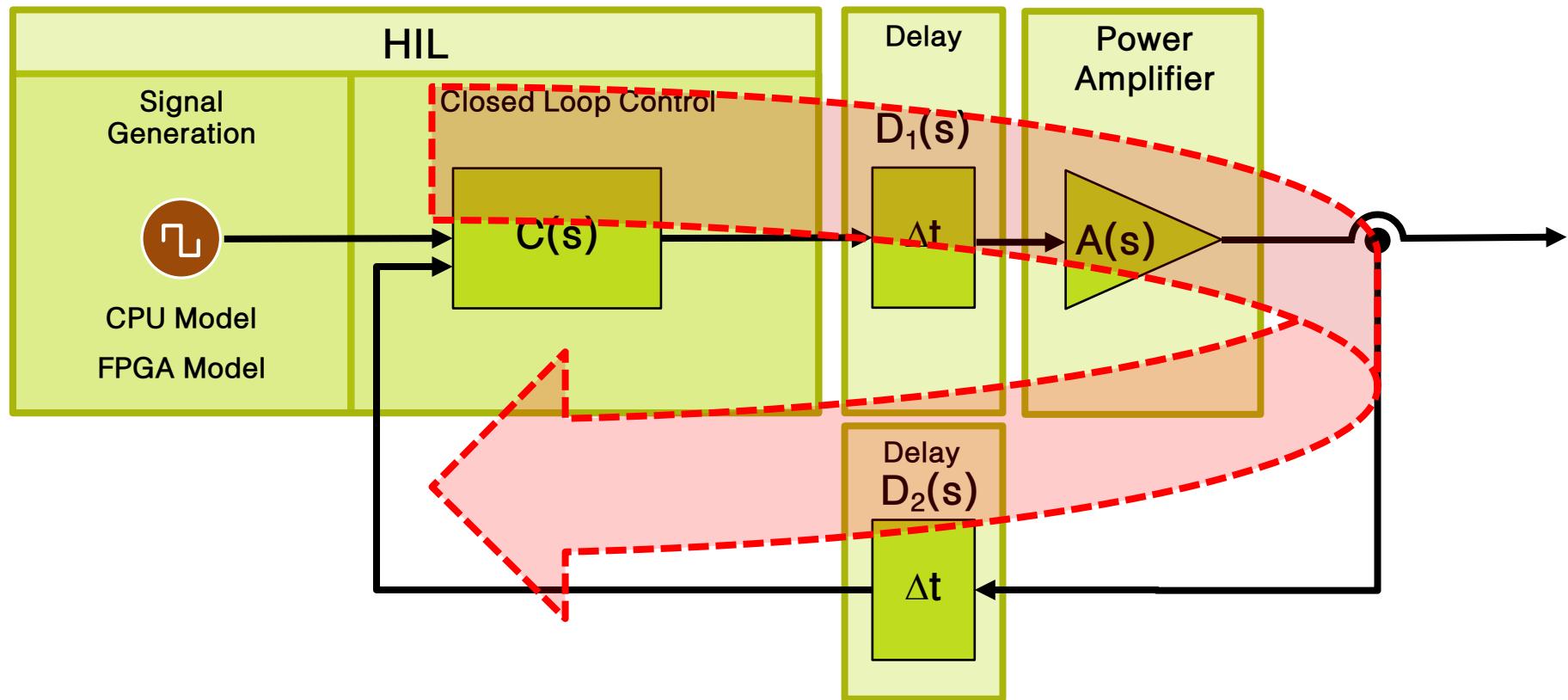
Delay & Phase Shift



Delay & Phase Shift

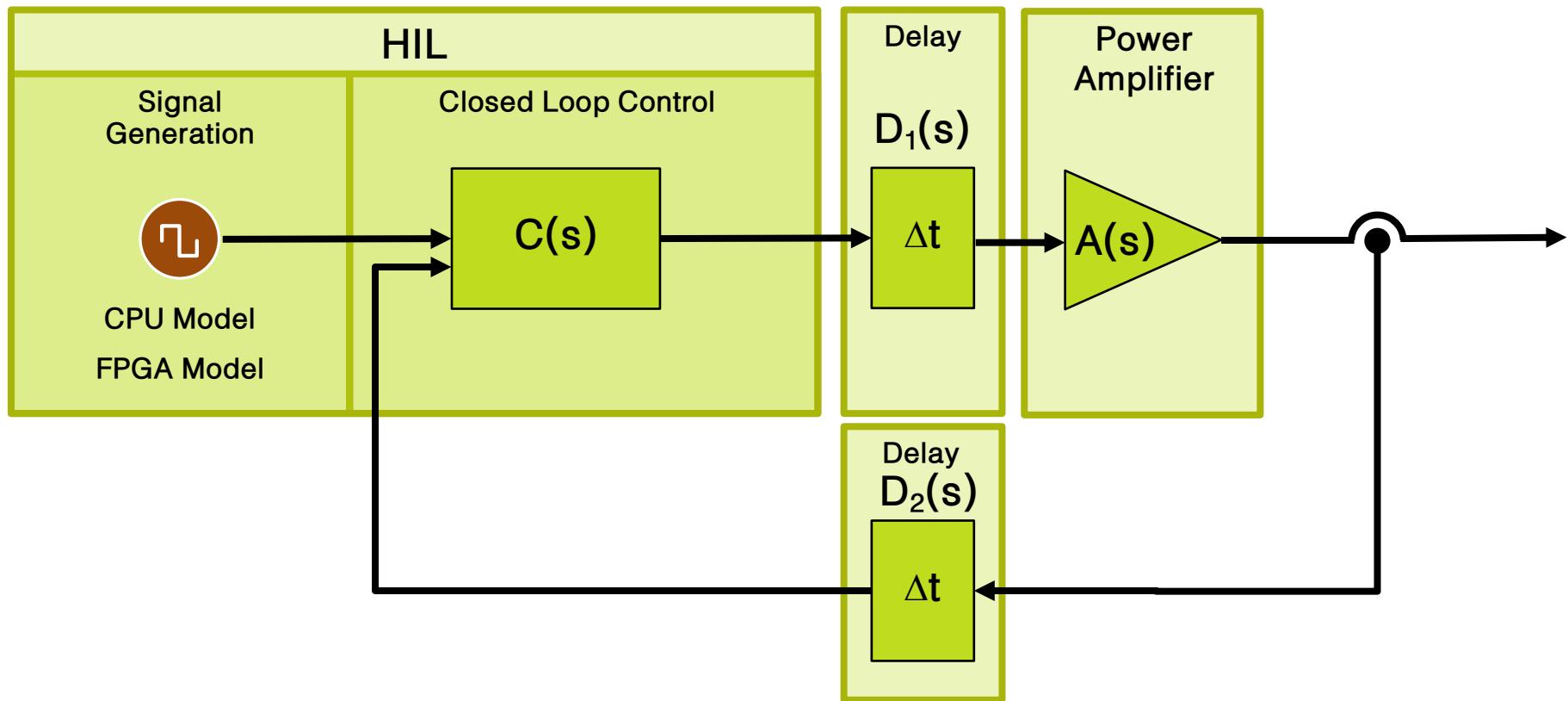


Stability Analysis – Open Loop Analysis



Stability Analysis

$$\frac{Y(s)}{X(s)} = \frac{C(s) \cdot D_1(s) \cdot A(s)}{1 + C(s) \cdot D_1(s) \cdot A(s) \cdot D_2(s)}$$



Stability Analysis

∴ Transfer Function Closed Loop

$$\frac{Y(s)}{X(s)} = \frac{C(s) \cdot D_1(s) \cdot A(s)}{1 + C(s) \cdot D_1(s) \cdot A(s) \cdot D_2(s)} = \frac{Z(s)}{1 + N(s)}$$

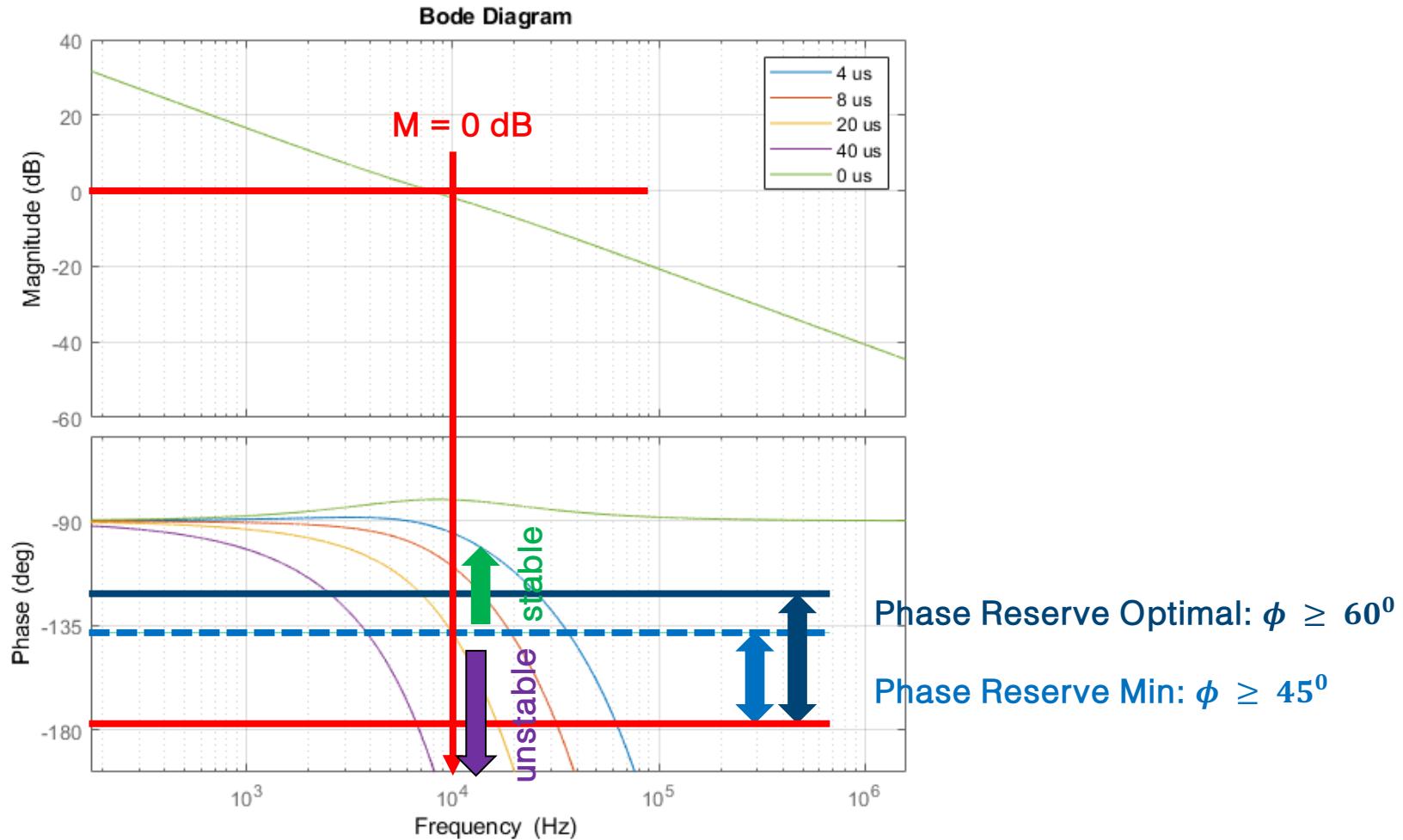
Instability: $1 = C(s) \cdot D_1(s) \cdot A(s) \cdot D_2(s) = N(s)$

$$Abs(N(s)) = 1 \rightarrow 0dB$$

$$\varphi = 180^\circ$$

Stability Criterion (Nyquist): Phase Reserve $\phi > 45^\circ$

Stability Analysis



REQ 6: Open Loop Delay

- ∴ Phase Shift & delay time: $\Delta t(f, \phi) = \frac{\phi}{360 \cdot f}$
- ∴ Nyquist: Open loop stability: At f_{Model_Max} Phase reserve $\phi > 45^\circ$

Suggestion: **Phase Reserve: $\phi \geq 60^\circ$**

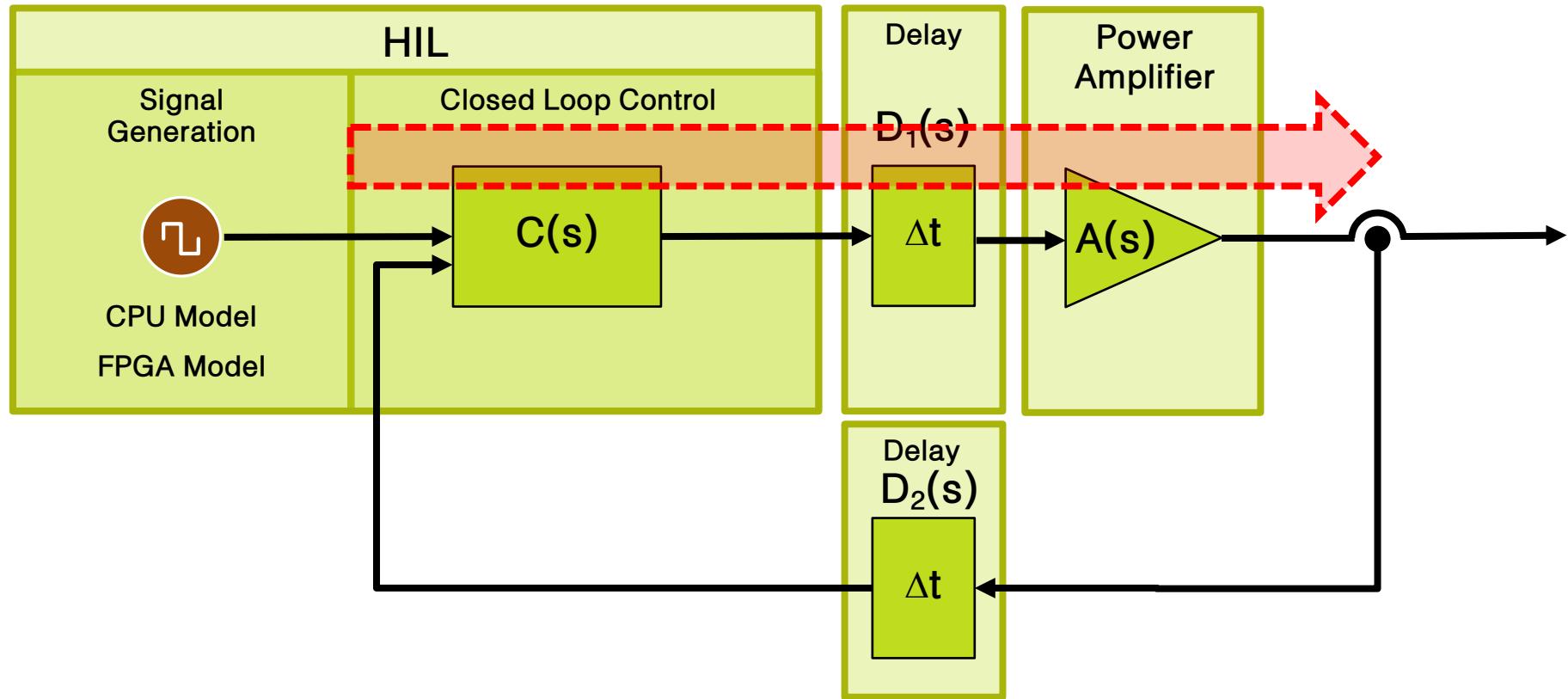
$$\phi = 180^\circ - \phi = 120^\circ$$

$$T_{Open_Loop_Delay}(f_{Model_Max}, 120^\circ) = \frac{120}{360 \cdot f_{Model_max}} = \frac{1}{3 \cdot f_{Model_max}}$$

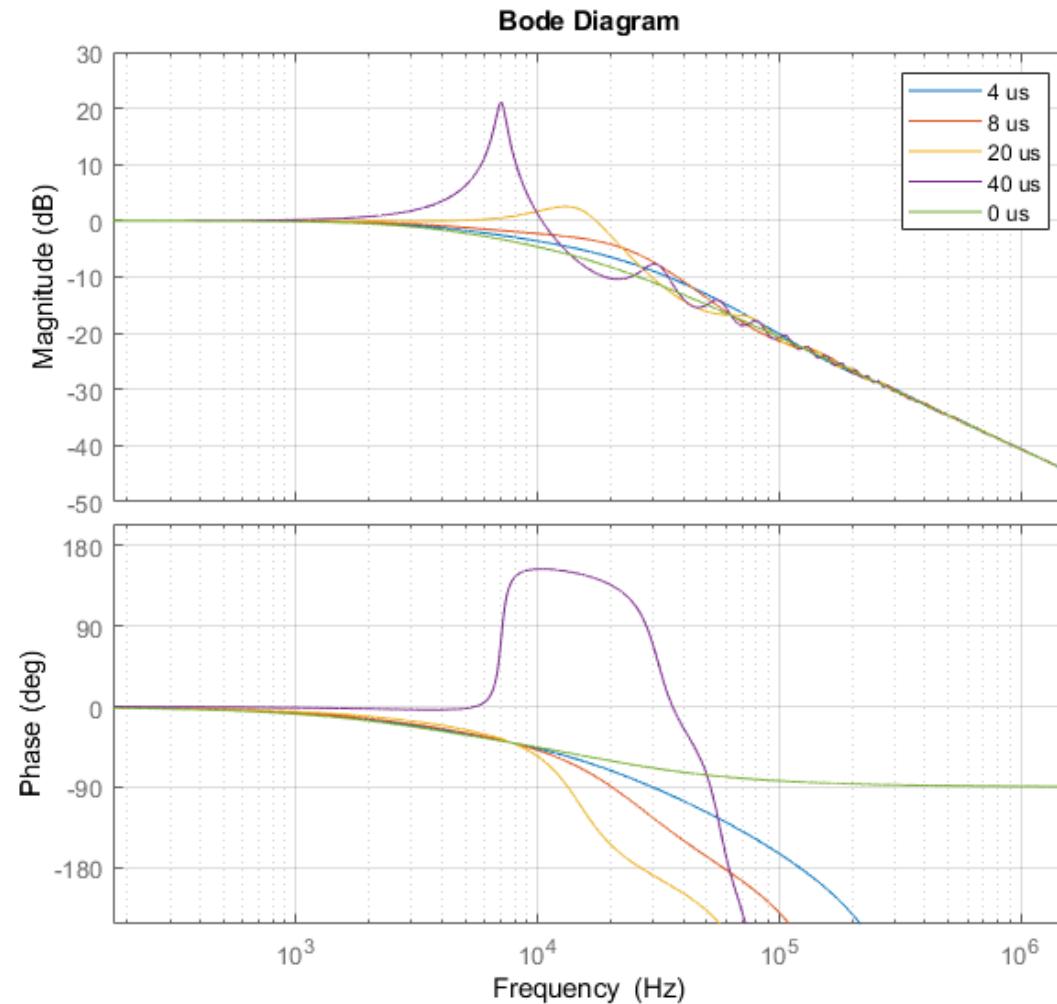
$$T_{Open_Loop_Delay} = T_{Transport_HIL_{Amp}} + T_{Amplifier} + T_{Transport_ADC_HIL}$$

REQ 6 Open Loop Delay: $T_{Open_Loop_Delay} < \frac{1}{3 \cdot f_{Model_Max}}$

Reference to Output



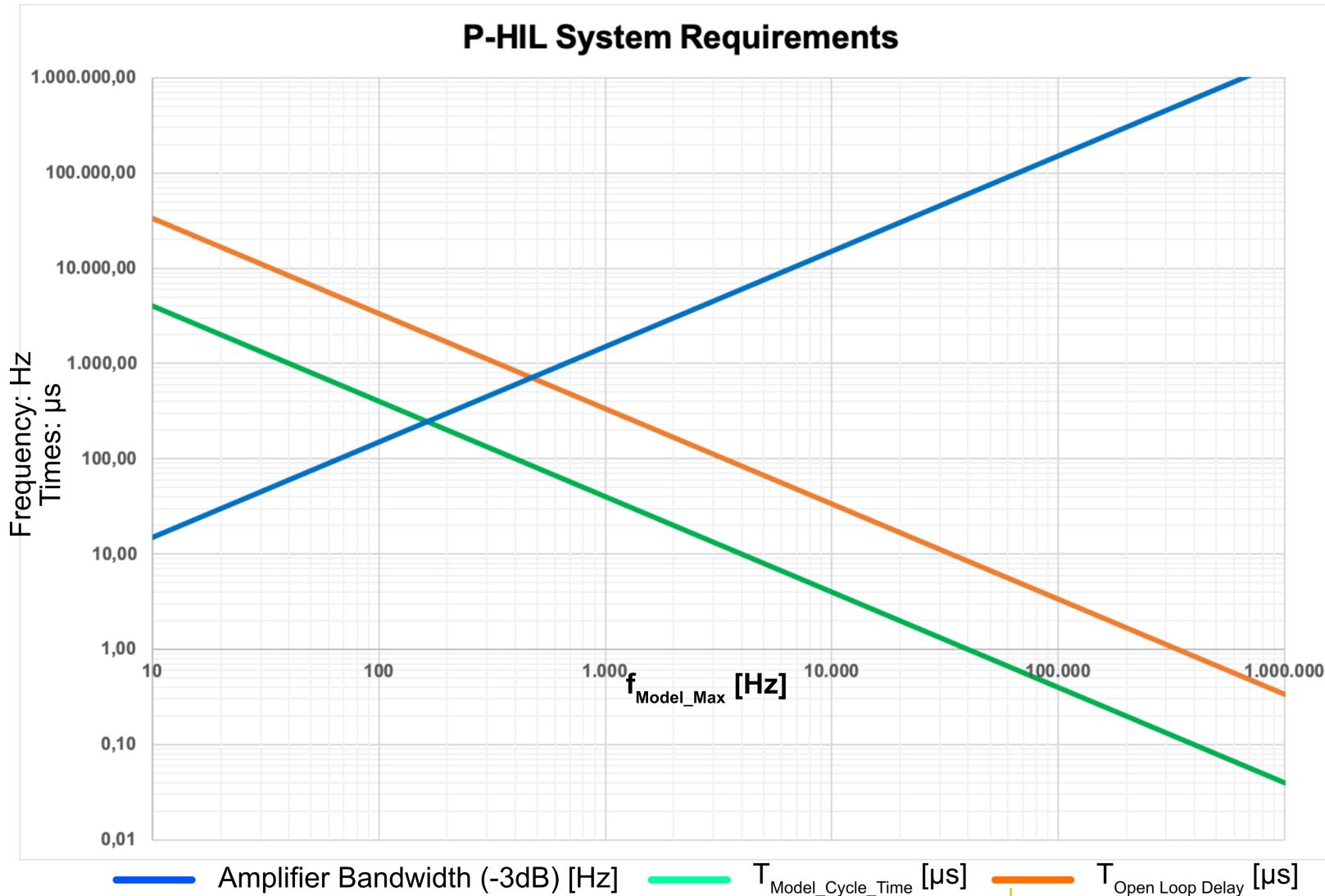
Reference to Output



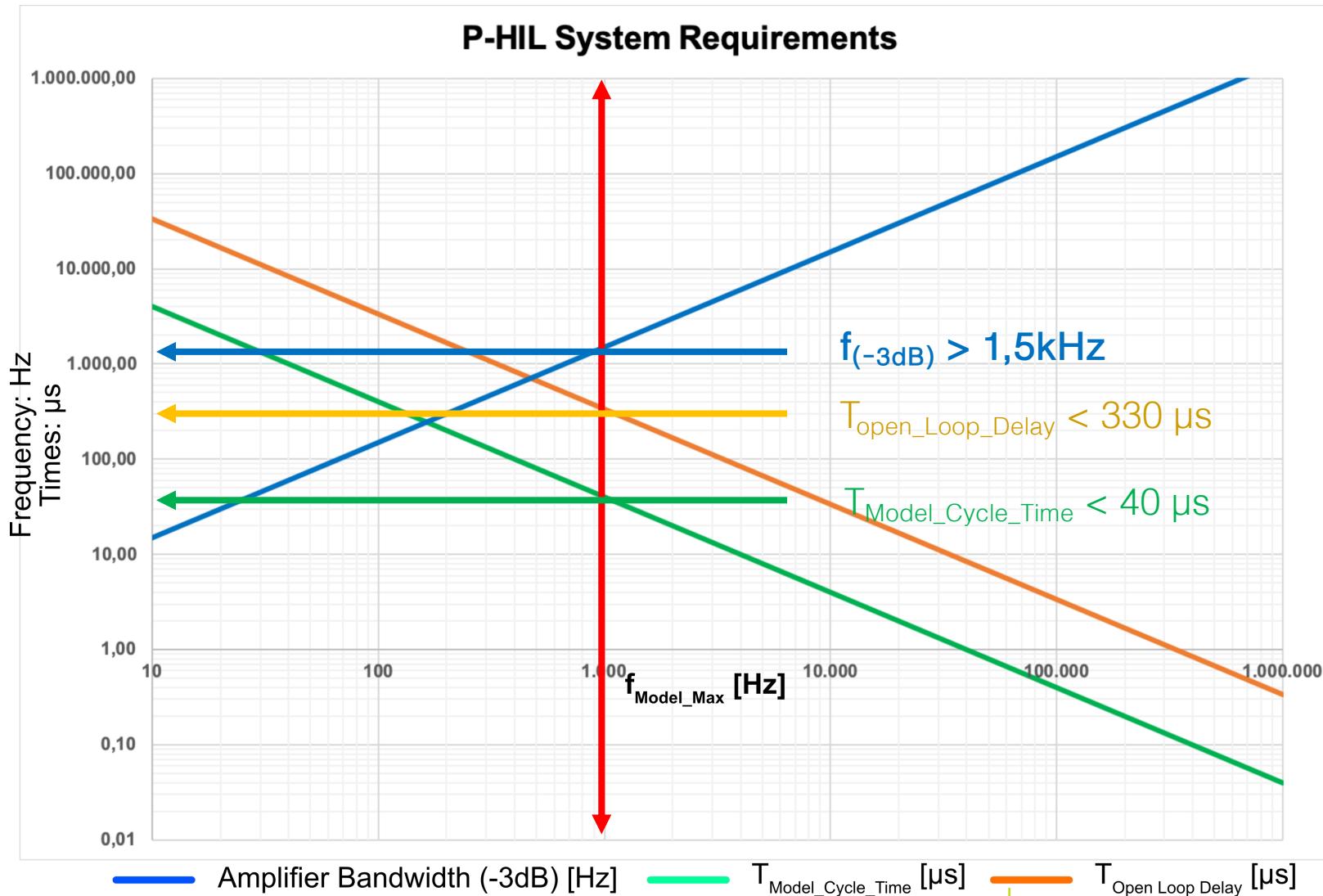
Summary REQ

- ..: REQ 1: define Maximum Model Frequency f_{Model_Max}
- ..: REQ 2: at least 25 set points per period @ f_{Model_Max}
- ..: REQ 3: $T_{Model_Cycle_Time} = \frac{1}{25 \cdot f_{Model_Max}}$
- ..: REQ 4: $T_{HIL_Cycle_Time} \leq T_{Model_Cycle_Time}$
- ..: Select Simulation Technology
 - $T_{HIL_Cycle_Time} > 4\mu s \rightarrow$ CPU Model
 - $T_{HIL_Cycle_Time} < 4\mu s \rightarrow$ FPGA Model
- ..: REQ 5: Amplifier Bandwidth (-3dB)
 - $f_{-3dB} > 1,5 \cdot f_{Model_Max}$
- ..: Phase Reserve: $\phi \geq 60^\circ$
- ..: REQ 6 Open Loop Delay: $T_{Open_Loop_Delay} < \frac{1}{3 \cdot f_{Model_Max}}$

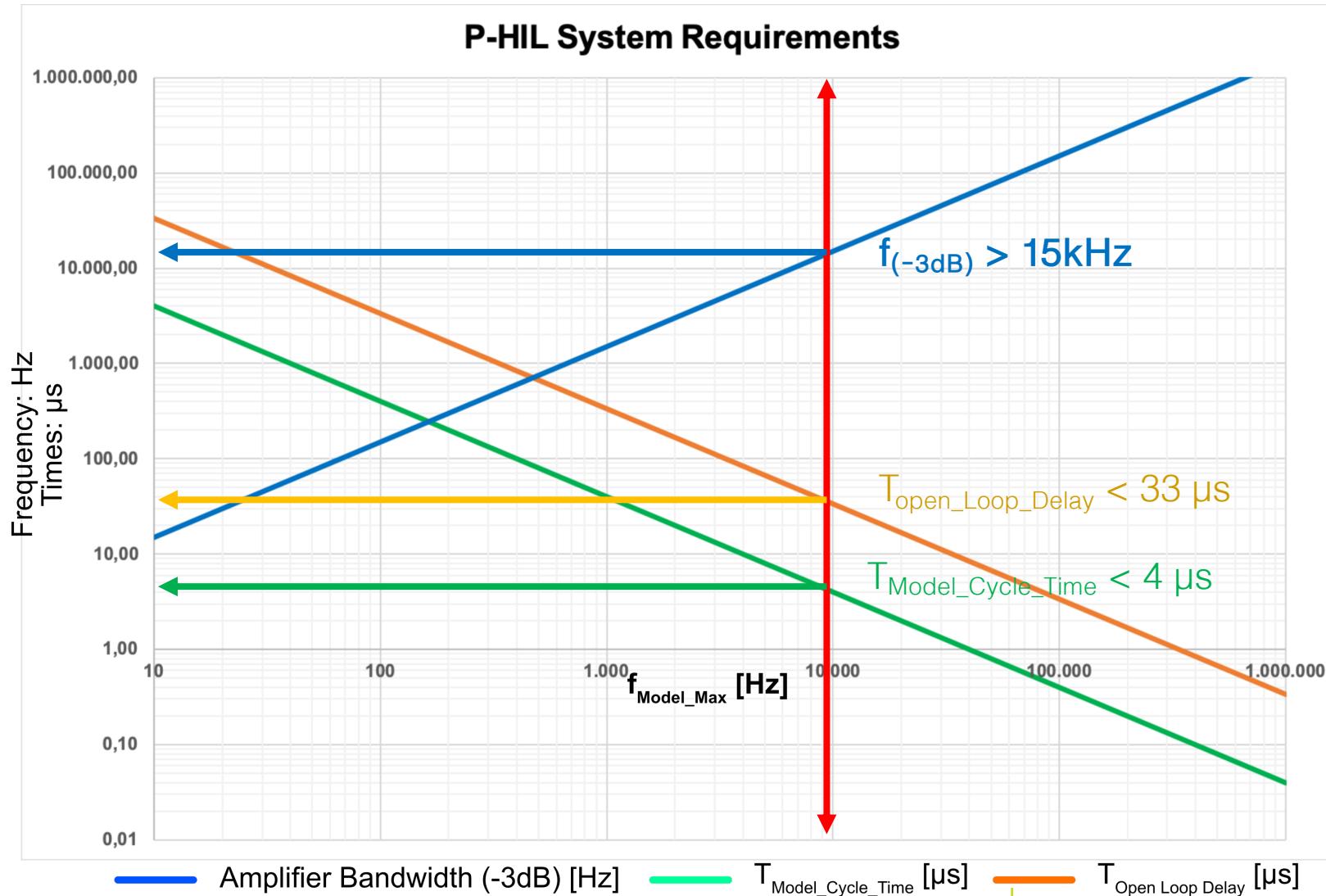
P-HIL Selection Table



Example: $f_{\text{Model_max}} = 1 \text{ kHz}$



Example: $f_{\text{Model_max}} = 10 \text{ kHz}$





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