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**European Research Infrastructure supporting Smart Grid   
Systems Technology Development, Validation and Roll Out**

Technical Report TA User Project

**PV Inverter characterization and power quality analysis**

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**All Authors/Partners** Manjunath Basappa Ayanna, CSIR

Van Hoa Nguyen, CEA INES

Quoc Tuan Tran, CEA INES

Marc Jung, CEA INES.

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**Abbreviations**

*TA* Trans-national Access

*CEA* Centre for Nuclear Energy and Alternative Energies

CSIR Council for Scientific and Industrial Research

EC Energy Centre

PV Photovoltaic

IEC International Electro-technical Commission

THD Total Harmonic Distortion

DUT Device under Test

MPPT Maximum Power Point Tracking

DC Direct current

AC Alternating current

Udc DC voltage

Idc DC current

Pdc DC Power

Uac AC voltage

Iac AC current

Pac AC power

PSI PV Simulator

CB Circuit Breaker

DA Data acquisition unit

GS Grid simulator

RLC Resistive, Inductive and Capacitive load

PA Power Analyzer

Umppmin Minimum power point tracking

Umppnom Nominal power point tracking

Umppmax Maximum power point tracking

Ƞconv Power conversion efficiency

Ƞconv EUR European power conversion efficiency

Ƞconv CEC Californian power conversion efficiency

Executive Summary

This report is generated as a deliverable for the ERIGrid Trans-national Access 5th call post proposal acceptance on the topic “PV Inverter characterization and power quality analysis” and after carrying out the various tests at the base station CEA-INES, France. The program is accessed for the period starting from 02 September 2019 to 01October 2019 including travel period. A commercially available inverter is characterized to gain hands on experience determining power conversion efficiency, measure the inverter response time during over / under voltage frequency situations and ride through functionality during short period voltage dips, measure harmonic distortions of a solar PV inverter connected to controlled load conditions for two different sky conditions and measure response time during islanded condition. The ERIGrid TA program offered a great platform to make use of the state-of-art test equipments where such an infrastructure is at large in a developing nation like South Africa, perform characterization tests under the guidance of the industry experts. The power conversion efficiency test carried out in accordance with EN50530 standard for normalized power conditions varying from 5% to 100% for minimum, nominal and maximum power point tracking values measured on an average 96%, 97% and 97% respectively. The European and Californian power conversion efficiency calculated as per the industry standard yielded 97% at nominal maximum power point. The response time of an inverter during over / under voltage or frequency tested as per IEC/EN 61727 standard with correct grid code set complied with the requirements stipulated for the various voltage and frequency levels. An experimental test carried out keeping the grid code parameters set to “Default” version and comparision of response time with South African grid code document NRS097-2-1 requirements revealed delayed response to trip during over / under voltage or frequency scenario. This finding is an interesting result where solar PV installers are prone to leave the grid code parameters set to default version mainly in small to medium scale rooftop PV applications during commissioning where the knowledge in this regard is limited. The over-ride functionality test for Y and X1 type of voltage dips performed as per the norm with the inverter functioning normally. The total harmonic distortions in current during two different sky conditions in accordance with IEC/EN 61727 measured distortions above the stipulated 5% during early morning and late afternoon periods where inverter tends to turn ON and OFF. On overall, the total harmonic distortions including odd orders 3rd to 9th, 11th to 15th, 17th to 21st and 23rd to 33rd on a cloudy sky measured higher distortions compared to clear sky irradiance profile. Due to time limitation, the response time to trip during one islanded test condition as per IEC/EN 62116 with -5% active power and 5% reactive power measured less than 2secs. The ERIGrid TA program provided a great platform to understand the inverter topology, set-up required test infrastructure, monitor the equipments, measure the required parameters, analyse and conclude few inverter characterization tests.

# General Information of the User Project

Project acronym:Solar photovoltaic (PV) Inverter characterization and power quality analysis

Project title: Inverter characterization, determine efficiency, conformance checks and measure harmonic distortions of a solar PV inverter connected to controlled loads at CEA, France

Host infrastructure: Centre for Nuclear Energy and Alternative Energies (CEA), INES, 17 Avenue Des Martyrs, Grenoble 38054

Access period: 02 Sep 2019 to 01 Oct 2019

User group member: Manjunath Basappa Ayanna

Council for Scientific and Industrial Research Energy Centre (CSIR EC) solar photovoltaic (PV) teams current capabilities include characterization of solar PV modules in indoor and outdoor conditions and develop storage devices including characterization for the ever growing renewable energy industry in the country as well as globally. There is a strong emphasis to increase localization content for PV components in the country and CSIR being a parastatal company supports the growth of local industry in all the respective sectors. Under the ERIGrid Trans-national Access (TA) program, we aimed to dive in more into technical aspects of solar inverter configurations, test infrastructure requirements and understand standards and protocols, real time characterization on different types of inverters, understand measurement uncertainties, analyze and publish results in the local / international conference. We also aimed to measure harmonic distortions induced by solar inverter under controlled loads. This access program is projected to increase our know-how and capability in the field of inverter characterization, to perform conformance checks in terms of efficiency, protection system as per national / international standards, measure and analyze harmonic distortions in controlled load conditions. It also enables us to expand our in-house solar PV testing facility capability to perform inverter characterization from the current PV modules and battery storage characterization capabilities. The CSIR EC solar PV testing facility will be a research platform for several students from various universities and supports the local developers and manufacturers towards increasing the localization of technologies in the country**.**

As part of ERIGrid TA program proposal acceptance, we planned to travel to CEA, get hands on experience on characterizing a solar inverter, measure all the required parameters under standard test conditions to calculate efficiency and understand the protection system at much higher levels. We aimed to utilize the programmable DC power supplies to simulate solar PV generation, load banks (RLC), AC power source (grid simulator) to simulate a low voltage power grid operation and power quality meters to analyse the response time during over/under voltage/frequency levels, measure harmonic emissions during different sky conditions levels and calculate the efficiency of the inverter at different load conditions. In the process we also planned to engage with the CEA leadership team to understand the measurement uncertainties, safety requirements, laboratory conditions, standard operating procedures, calibration requirements, remote control and data acquisition etc.

# Research Motivation

Grid-tied PV systems are the fastest growing renewable energy source for power generation today. The quality of the electricity produced from PV directly depends on the amount of solar irradiance. Changes in weather conditions, rainfall and cloud movements affect the output power from PV. The primary reason for variable output power from PV is due to cloud movements. These power fluctuations on a grid-tied low voltage network also causes harmonic distortions in current waveforms [1]. PV inverters are the main source of injecting current harmonics into the network. The injected harmonics can increase power losses in the system [2]. There’s a motivation worldwide to conduct power quality analysis as more embedded generators particularly solar PV systems are connected to low voltage utility grid. High penetration of intermittent PV cause voltage fluctuations in grid, voltage rise and reverse power flow, power fluctuations in grid, variation in frequency and grounding issues. PV penetration in low voltage distribution network also causes harmonic distortion in current and voltage waveforms [3]. Power quality analysis includes harmonic distortions, reverse power flow, voltage fluctuations and power fluctuations. These parameters must comply with the governing standards in order to ensure the safe operation of connected loads and cleanliness of the supply. In South Africa, the solar PV modules characterization is carried out only at CSIR EC, Pretoria and Nelson Mandela University, Port Elizabeth. CSIR EC houses the country’s first solar PV reliability test lab which includes climatic chambers, sun simulator, mechanical load tester, outdoor IV characterization systems etc. We have already ear-marked space in our existing solar PV reliability laboratory for developing solar PV inverter test infrastructure and support the local PV industry.

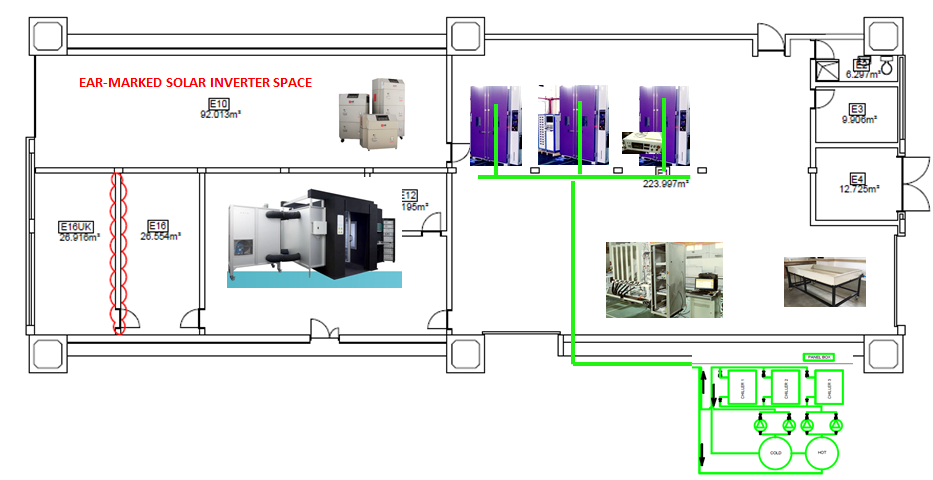


Figure 1: CSIR Solar PV Indoor Reliability laboratory layout diagram

The proposed inverter test facility at our premises will be a research platform for many students to carry out research on locally developed power converters. Under the ERIGrid TA access program, we aimed to expand our knowledge base and capability in the field of inverter characterization and establish test and research facility in the country. Furthermore, the confidence of customers and the general public into the PV technology could be strengthened by supplying locally compiled test data and results.

We foresee the below potential benefits from our solar PV testing facility (mainly PV modules and inverters):

* Developing competencies in the development of solar energy technologies
* Training & development of the necessary manpower to design, construct, operate and maintain PV power plants
* In-country training of personnel for renewable energy projects : Engineers, in collaboration with Universities, Technicians and technologists, in collaboration with Universities of Technology, Specialist artisans, in collaboration with Further Education and Training (FET) colleges
* To contribute in the development of a new generation of trained scientists at PhD, Masters and Honours levels

The establishment of the test facility at the CSIR would mean that new technologies can be tested locally instead of sending them to other facilities overseas. This would have the advantage of:

* Elimination of the requirement for international travel, which results in greatly reduced transport costs and the ability to utilize or train larger numbers of people for longer periods of time for an existing budget
* Shorter lead times for travel, as personnel do not require visas and equipment does not have to pass through customs
* The ability to expose non-specialists such as decision-makers, journalists and schoolchildren to in-country developments
* It will allow for greater flexibility by not being reliant upon testing schedules at foreign facilities
* The facility will provide the freedom to pursue work in the South African interest, without being constrained by the interests or capabilities of foreign institutions' staff or facilities

The successful completion of technical exposure at CEA-INES under ERIGrid TA program will enable us to develop our skills in inverter characterization domain. This also enhances our capability in the country to establish and provide end to end testing solutions for all the local manufacturers. The test facility will be a platform for all the research students in the country. The subjection of inverter to controlled load conditions and analyzing the power quality parameters will be a new experience and forms a platform for future research in the organization.

## Objectives

Due to significant drop in PV prices, many consumers are switching to embedded generation to reduce the ever increasing electricity tariffs in the country. South African utility company has raised concerns about the un-safe inverter operations during low voltage grid network maintainace periods. Also there are concerns of increased injection of harmonic levels due to high frequency switching devices (inverters) coming in-line into the low voltage grid network. The objective of this project is to mainly increase our know-how and capability in the field of inverter characterization within the country and further carry out detailed research on power quality issues with embedded generation.

## Scope

Characterize a solar inverter to determine efficiency, perform anti-islanding tests, measure the inverter response time during over / under voltage frequency situations and measure harmonic distortions of a solar PV inverter connected to controlled load and gird conditions at solar PV laboratory, CEA-INES, Le Bourget Du Lac, France

# State-of-the-Art/State-of-Technology

The lack of infrastructure for inverter characterization in the country drove us to submit the proposal to access the ERI Grid TA program and characterize the inverter in terms of over / under voltage and frequency trip time, voltage ride through test and perform efficiency related measurements at CEA-INES France in accordance with IEC/EN 61727 [4], IEC/EN 62116 [5], EN50530 [6] and South African document NRS097-2-1[7]. It was also proposed to run few test on harmonic measurements under controllable load conditions. These test activities are supposed to enhance our knowledge to conduct further research in this domain.

# 

# Executed Tests and Experiments

The following tests are carried out in conjunctions with the proposal document on a widely available commercial 3ph 25kWp inverter in the market. The tests are carried out only to get hands on experience in the field of inverter characterization and the results obtained in this study are only for learning purpose and does not certify any product operations.

* Determination of Power conversion efficiency (European and California efficiency)
* Determination of trip time of an inverter during over / under voltage situations (Default and EN 61646 grid code settings)
* Determination of trip time of an inverter during over / under frequency situations (Default and EN 61646 grid code settings)
* Check Inverter ride through functionality during under voltage situations for very short durations
* Determine Total Harmonic Distortions (THDi) for the current for a clear and cloudy day irradiance profile
* Inverter response time during islanding conditions (Generation to load ratio at -5% and + 5% in active and reactive power respectively)

## Test Plan

* The following test plan is derived to execute the earlier mentioned tests. Prior to my arrival at the CEA-INES facility, it is pre-agreed between both the parties to use the available inverter and other lab equipments at the CEA-INES. No test components or measuring equipments are carried from CSIR.
* The scope and type of tests to be carried out at CEA-INES is determined from the ERI Grid project proposal document.
* It is decided that all the major operations or infrastructure establishments for the tests to be carried out will be done by CEA personnel as per the organisation policy.
* The required skills to carry out the tests are assessed and the availability of the personnel during the project period is assessed. Planning in advance is carried out to keep the tests running during the absence periods of the respective lab personnel.
  + Mr. Van Hoa Nguyen is the mentor/supervisor during the course of the project.
  + Mr. Marc Jung is assigned as laboratory technician to perform all the electrical infrastructure assembling and interconnection of components
  + I am responsible to determine the type of test, conceptualize, draft test conditions, run the tests, data retrieval, analyse, calculate and compare the measured results against the requirements stipulated in standards.
* The environment conditions such as maintaining the required laboratory temperature and barricading the test space to prevent un-authorized entry is done.
  + Safety induction training is provided to me prior granting the access to the laboratory.
* The monitoring parameters for each of the test are identified from IEC/EN 61727, IEC 62116 and EN 50530.
* A test schedule is planned for all the working days during my 4 weeks stay period at the facility. Sufficient time is allocated to organise the required equipments and prepare the test infrastructure for each of the test. Table 1 presents weekly schedule to run the planned tests at the base station and complete reports post return to CSIR.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Wk 1 | Wk 2 | Wk 3 | Wk 4 | Wk 5 | Wk 6 |
| Power Conversion Efficiency test |  |  |  |  |  |  |
| Over / Under voltage tests |  |  |  |  |  |  |
| Over / Under frequency tests |  |  |  |  |  |  |
| Ride through functionality tests |  |  |  |  |  |  |
| Harmonic measurements tests |  |  |  |  |  |  |
| Islanding tests |  |  |  |  |  |  |
| Data analysis |  |  |  |  |  |  |
| Report generation |  |  |  |  |  |  |

Table 1: Inverter characterization test schedule

* Method of the communications during the project is planned and decided mostly to be a verbal communications and always working together with Mr. Van Hoa Nguyen and Mr. Marc Jung. Email interactions whenever required.

## Standards, Procedures, and Methodology

During proposal phase, it was mentioned that inverters would be tested against South African NRS097 standard. As the Device under Test (DuT) is a commercially available product in France and as the technical exposure under this project is to understand the technicalities involved during inverter characterization, IEC/EN 50530 and IEC/EN 61727 standards are widely used to determine the test sequence, criterions and evaluate the measured results.

* Power Conversion Efficiency test:
  + Note the Umppmin, Umppnom and Umppmax voltage of the DuT from rating label.
  + For each Maximum Power point Tracking (MPPT) voltage level, power conversion efficiency parameters are measured at 8 power levels (5%, 10%, 20%, 25%, 30%, 50%, 75% and 100%) normalized to the rated power.
  + Determine the solar irradiance (W/m2) for the PV simulator using PRISMES software by feeding the calculated current, Idc for Umppmin, Umppnom and Umppmax values.
  + A measurement dwell period of 10 minutes is considered for each of the power levels with 5 minutes of interval between the measurements.
  + Prepare an irradiance profile for the each of the MPPT voltage and load it to PV simulator and wait untill the inverter synchronizes with the grid.
  + Monitor the entire system for steady operations during the test period.
  + Record the measured values of Udc, Idc, Uac and Iac at an interval of every second.
  + The power conversion efficiency (Ƞconv) from the i*,* simultaneous measurements of Udc, Idc, Uac and Iac over a period ∆T as per the equation (1).
    - = (1)
  + The European power conversion efficiency (ȠconvEUR) and Californian power conversion efficiency (ȠconvCEC) can also be calculated using the equations (2) and (3).

ȠconvEUR = 0.03Ƞconv,5% + 0.06Ƞconv,10% + 0.13Ƞconv,20% + 0.1Ƞconv,30% + 0.48Ƞconv,50% + 0.2 Ƞconv,100% (2)

ȠconvCEC = 0.04Ƞconv,5% + 0.05Ƞconv,10% + 0.12Ƞconv,20% + 0.21Ƞconv,30% + 0.53Ƞconv,50% + 0.05 Ƞconv,100% (3)

* Over / Under Voltage and Frequency test (IEC/EN 61727 Grid code parameter set on DuT):
  + To test the inverter for IEC/EN 61727 Metropolitan Electricity Authority (MEA) requirements: Manually adjust the Rotary switch A to position B and Rotary switch B to position 8 on the inverter underneath the LCD display board to set the right grid parameters compliant to IEC 61727. This can also be set remotely using dedicated portals by respective manufacturers.
  + Design a logic diagram using Simulink tool on MATLAB to run the test in steps.
  + Program the test steps for the below mentioned voltage and frequency levels allowing sufficient time in-between for the inverter to turn ON post dis-connection from the grid.
  + Apply stable DC input from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.
  + Allow some time for the inverter to synchronize with the grid parameters and turn ON.
  + Monitor the entire system for steady operations during the test period.
  + Record the real time voltage and current for all the 3 phases and frequency values at every 50µS time intervals and analyse the measured values.
  + Determine the response/trip time and verify against the values stipulated in the standard.

|  |  |
| --- | --- |
| **Voltage Range (At PoC)** | **Response / Trip time (secs)** |
| V < 50% | 0.1 |
| 50% ≤ V <85% | 2.0 |
| 85% ≤ V ≤ 110% | Continuous operation |
| 110% < V < 135% | 2.0 |
| V ≥ 135% | 0.05 |
| **Frequency Range** |  |
| 49 Hz to 51 Hz | 0.2 |

Table 2: Voltage and Frequency test range per EN 61727

* Over / Under Voltage and Frequency test (Grid code parameter set to Default on DuT):
  + An experimental test is carried out by keeping the grid code setting in Default setting (Rotary switch A and B at position 0) and compare the response time of an inverter against NRS 097-2-1:2017 requirements. This exercise is to understand the inverter response time during over or under voltage / frequency conditions when an installer leaves the grid parameter setting under default condition during commissioning (can happen mostly in developing countries like South Africa or any other).
  + Design logic diagrams and program the test steps as explained in the earlier test for EN61727 grid code setting.
  + Apply stable DC input from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.
  + Allow some time for the inverter to synchronize with the grid parameters and turn ON.
  + Monitor the entire system for steady operations during the test period.
  + Record the real time voltage and current for all the 3 phases and frequency values at every 50µS time intervals and analyse the measured values.
  + Determine the response/trip time and verify against the values stipulated in the standard.

|  |  |
| --- | --- |
| **Voltage Range (At PoC)** | **Response / Trip time (secs)** |
| V < 50% | 0.2 |
| 50% ≤ V <85% | 10 |
| 85% ≤ V ≤ 110% | Continuous operation |
| 110% < V < 115% | 40 |
| 115% ≤ V < 120% | 2 |
| V ≥ 120% | 0.16 |
| **Frequency Range** |  |
| <47 Hz | 0.2 |
| 47 ≤ Hz ≤ 50.5 Hz | Continuous operation |
| 50.5 ≥ Hz ≥ 52 Hz | Active power shall not increase and shall drop at a gradient of 50% per Hz |
| >52Hz | 0.5 |

Table 3: Voltage and Frequency test range per NRS097-2-1

* Ride through functionality test:
  + Design a logic diagram using Simulink tool on MATLAB to run the test in steps.
  + Program the test steps for the below mentioned voltage ride through levels allowing sufficient time for the inverter to turn ON post dis-connections from the grid if any.

|  |  |  |
| --- | --- | --- |
| **Dip type** | **Ride through voltage levels** | **Duration** |
| Y type | 10% ≤ V ≤ 15% | 2000 ms |
| Y type | 15% ≤ V ≤ 20% | 600 ms |
| Y type | 20% ≤ V ≤ 30% | 150 ms |
| X1 type | 30% ≤ V ≤ 40% | 150 ms |

Table 4: Voltage ride through range per EN61727

* + Apply stable DC input from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.
  + Allow some time for the inverter to synchronize with the grid parameters and turn ON.
  + Monitor the entire system for steady operations during the test period.
  + Record the real time voltage and current for all the 3 phases and frequency values at every 50µS time intervals and analyse the measured values.
  + Determine the response/trip time and verify against the values stipulated in the standard.
* Harmonic measurements:
  + Perform measurement of Harmonic distortions in the current waveform for a full clear and cloudy sky day conditions. This test is also conducted without any load connected in the circuit.
  + Design a logic diagram using Simulink tool on MATLAB to run the test continuously and load it to the grid simulator.
  + Install a power quality analyzer and connect the voltage and current measurement probes of the Power Analyzer (PA) to the inverter output terminations.
  + Prepare solar irradiance profile consisting 30 sec interval for a full day and program the PV simulator to feed the DC power continuously based on the irradiance.

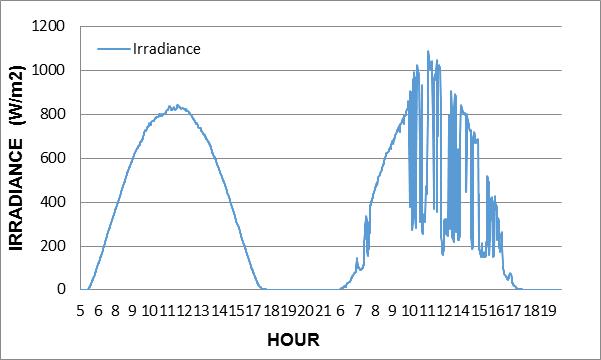


Figure 2: Solar Irradiance profile for clear and cloudy sky conditions

* + Keep the per phase AC power output limited to 4000W totalling to 12000W feeding to the grid.
  + Calculate the Resistance (R), Inductance (L) and Capacitance (C) values for the RLC load bank using below equations and apply it to the load bank.

R = V2 RMS / P (4)

L = V2RMS / 2πfPQf (5)

C = PQf / 2πfV2RMS (6)

Where Qf = R = 1

* + Apply the programmed DC voltage and current inputs based on solar irradiance data from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.
  + Monitor the entire system for steady operations during the test period.
  + Record the voltage, current, frequency and harmonic emissions upto 50th order (3kHz) at every second interval.
  + Analyze and calculate the Total Harmonic Distortions (THDi) and Odd/Even harmonics for multiple orders for the current using the equation (7)

THDi = (7)

* + Verify the measured values against the requirements stipulated in EN 61727 as per Table (5)

|  |  |
| --- | --- |
| **Odd harmonics** | |
| 3rd to 9th | Less than 4.0% |
| 11th to 15th | Less than 2.0% |
| 17 to 21st | Less than 1.5% |
| 23rd to 33rd | Less than 0.5% |
| **Even harmonics** | |
| 2nd to 8th | Less than 1.0% |
| 10th 32th | Less than 0.5% |
| **Total harmonics** | Less than 5% |

Table 5: Maximum allowed harmonic levels as per IEC/EN 61727

* Islanding test:
  + IEC/EN 62116 standard stipulates to subject the inverter to an islanding condition with active and reactive power test conditions (%) ranging as per the below table and at >90%, 50%±10% and <10% of the rated Vmpp.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Active and Reactive power test conditions (%)** | | | | |
| -10,10 | -5,10 | 0,+10 | 5,10 | 10,10 |
| -10,5 | -5,5 | 0,+5 | 5,5 | 10,5 |
| -10,0 | -5,0 | 0,0 | 5,0 | 10,0 |
| -10,-5 | -5,-5 | 0,-5 | 5,-5 | 10,-5 |
| -10,-10 | -5,-10 | 0,-10 | 5,-10 | 10,-10 |

Table 6: Generation to load active and reactive power range

* + The test passes if both the following results for the recorded run-up time are satisfied:
    - It has to be less than 2s in each transient;
    - Each unbalanced condition of the grey shaded area of Table (6), it has to be less than that in the balanced one (cell 0, 0); if not, the tests must be extended to the un-grey shaded area.
  + Due to limitation in time, only one test condition scenario where active power of generation to load is -5% and reactive power at +5% is simulated and tested.
  + In this test, the per phase AC power output is limited to 3000W totalling to 9000W in the system.
  + Calculate the Resistance (R), Inductance (L) and Capacitance (C) values for the RLC load bank using the equations (4) (5) and (6) and apply it to the load bank.
  + Design a logic diagram using Simulink tool on MATLAB to run the test with a possibility to cut the power supply from the grid and load it to the grid simulator.
  + Inject a stable DC power from the PV simulator to the inverter to keep the inverter synchronised and feeding power to the loads continuously.
  + Trigger a grid failure situation using OPAL-RT real time simulation software and create an islanded condition with the active and reactive power levels at -5% and 5% respectively.
  + Monitor the entire system for operation and record the AC voltage, AC current, active and reactive power on 50µS intervals and analyse the measured results.
  + Determine the response time post grid failure and verify against the values stipulated in the standard.

## Test Set-up(s)

The following equipments are used to perform the mentioned tests in section 4:

* DC power supply Elektro Automatic PSI 91500-30

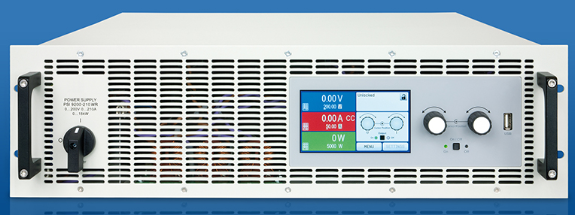


Figure 3: DC Programmable Power Supply Unit / PV simulator

* Technical specs: 15 kW max each, PV simulator function included (possibility to simulate irradiance fluctuation), 1500 VDC max, 30 A DC max.

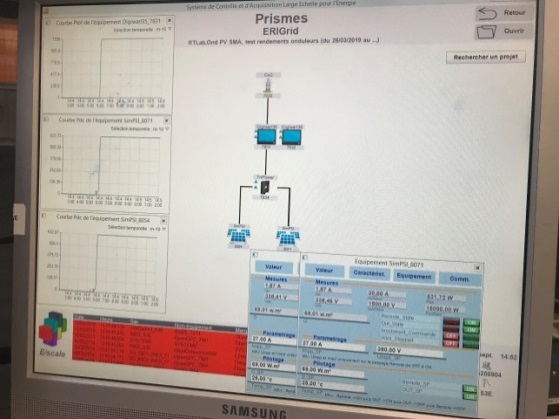


Figure 4: Prismes software for PV Simulator

* PRISMES software is used to configure, remote monitoring, control and data acquisition purposes for PSI. Additional PSI’s are looped together to supply power to multiple MPPT’s at the same time where the test conditions demanded for full load conditions.
* 400V 3 ph+N Grid simulator

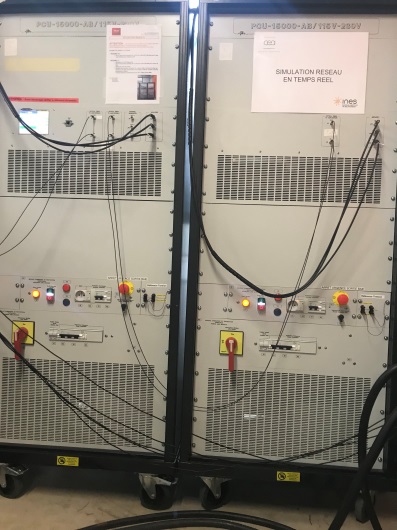


Figure 5: 3ph 15kVA Grid simulator

* Technical specs: 45 kVA generation (from simulator to EUT), 15 kVA absorption (from EUT to simulator), the simulator can be autonomous or driven by an OPAL RT system, Voltage AC range: from 120V to 690V, Frequency range: from 0 to 2500 Hz, Possibility to inject voltage harmonics
* OPAL-RT simulation software that provides powerful, real-time simulation solutions for electrical conversion, enabling customers to more quickly conduct precise and exhaustive testing on all controls is used to drive the grid simulator and conduct the tests
* Solar inverter - Device under Test (DUT)
* The device under test is a commercially available product with 3 phase 25kWp power output.
* Electronic Load (RLC)



Figure 6: Electronic Load / RLC load bank

* Technical specs: 30 kVA, 40 ARMS, Consumption of AC 3-phase or 1-phase current -100% configurable power factor, inductive and capacitive, Configurable harmonics, Operation modes: CC, CP and CI, Automatic test from Excel file.
* An Ethernet communication interface with protocol MODBUS/TCP is used to configure, monitor and operate the electronic load. By using HMI software application provided by CINERGIA, uploading of excel files is also possible.
* Power Analyzer



Figure 7: Power Analyzer

* + Technical specs: TRMS AC+DC voltage up to 1,000 V, TRMS AC+DC current: 5 mA to 10 kA depending on the sensors, Frequency, Power values: W, VA, var, VAD, PF, DPF, cos φ, tan φ, Energy values: Wh, varh, VAh, VADh, BTU, toe, Joule, Harmonics from 0 to the 50th order, phase Transients: up to 210, Inrush with waveform over a period > 10 minutes, True Inrush function, Recording of a selection of parameters at the maximum sampling rate for several days to several weeks Alarms: 10,000 of 40 different types, Peak detection Vectorial representation, USB communication, IEC 61000-4-30 Class B
  + The measurements obtained are processed using PAT software tool delivered as standard package. They allow configuration, transfers, processing and analysis. In addition, Data view® is available as an option and offers the possibility of generating reports according to the voltage quality standards.
* Monitoring
  + The operation of all the equipments and functioning of the DuT is physically monitored on real time where the test duration is short. For the harmonic measurement test which is for full day solar irradiance profile and for different conditions, the operation of the equipments is remotely monitored. All the DC data including voltage and current is acquired by PRISMES software and the AC part including voltage, current, frequency, power factor with other key electrical parameters are acquired by OPAL-RT software.
* The below single line diagrams presents the equipments including DuT used to carry out the proposed tests in this project.
* Efficiency test, Over / Under voltage and frequency, Ride through test setup

DUT

PSI

---

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CB / DA

GS

**DC VOLTAGE AND CURRENT DATA ACQUISITION**

**AC VOLTAGE, CURRENT, FREQUENCY DATA ACQUISITION**

Figure 8: Single line diagram for efficiency test, over / under voltage and frequency and ride through test

* Harmonic measurements test set up

DUT

PA

PSI

---

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CB / DA

GS

**DC VOLTAGE AND CURRENT DATA ACQUISITION**

**AC VOLTAGE, CURRENT, FREQUENCY, HARMONICS UPTO 50TH ORDER**

RLC

Figure 9: Single line diagram for Harmonic measurements

* Anti-Islanding test set

DUT

PSI

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CB / DA

GS

**DC VOLTAGE AND CURRENT DATA ACQUISITION**

**AC VOLTAGE, CURRENT, FREQUENCY, ACTIVE AND REACTIVE POWER DATA ACQUISITION**

RLC

Figure 10: Single line diagram for anti-islanding test

## Data Management and Processing

* Power conversion efficiency test:
* Solar irradiance data with the Udc, Idc and Pdc are averaged to every minute interval from their measured data at every 30 seconds interval in the first step.
* In the next step, the Uac and Iac for all the 3 phases are averaged to every minute interval from their measured data at every second interval.
* Based on the data sets and time stamp match, the measured calculate the DC data is aligned with the measured AC data on a MS spreadsheet.
* The power conversion efficiency is calculated from the sum of AC and DC power values as per the Eq. (1) for minimum, rated and maximum MPPT voltages. The European and Californian efficiency are also calculated as per Eq. (2) and (3).
* Over / under voltage and frequency, ride through functionality tests:
* In this test, the Uac, Iac, Hz are the critical parameters to determine the trip time of an inverter. These parameters are monitored at 50µS interval for all the 3 phases.
* The acquired data is processed using MATLAB software and simple scripts to plot the Uac, Iac and Hz for the same time frame.
* Measured Iac is used as common metric against varying voltage and frequency to determine the trip time.
* The measured Uac is plotted followed by Iac for the same time frame and similarly measured Hz followed by Iac.
* The time taken to trip or override the different set of conditions is calculated from the Iac curve.
* Harmonics measurements test:
* Solar irradiance data with the measured Udc, Idc and Pdc are averaged to every minute interval in the first step.
* The data stored on the Power analyzer memory space is downloaded to MS spreadsheet version.
* Based on the datasets and time stamp match, the irradiance, Uac, Iac, Pac are averaged to 1 minute interval using pivot table for all the 3 phases.
* The harmonic emissions in each phase for the range of orders mentioned in table (5) are calculated on an hourly basis as per the equation (7).
* Islanding test:
* In this test, the generated power is carefully balanced with the demand by the load considering active power and reactive power values to be as per Table (6).
* The Uac, Iac, for all the 3 phases with active and reactive power data is monitored and recorded at 50µS interval.
* The acquired data is processed using MATLAB software using simple scripts to plot the Uac, Iac, active and reactive power at the same time frame.
* The trip time is calculated based on the Iac values in an islanded condition.

# Results and Conclusions

* Power conversion efficiency test
* The power conversion efficiency (Ƞconv) is carried out as per the methodology briefed in section 4.2. Figure 11 presents the calculated efficiency from the measured DC and AC power for Umppmin, Umppnom and Umppmax.

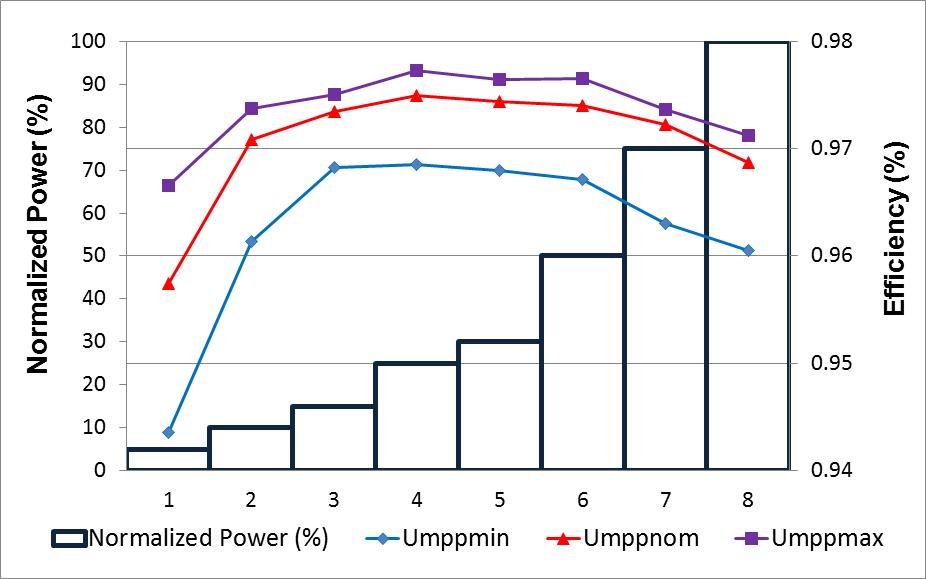


Figure 11: Power conversion efficiency measured at min, nom and max MPPT voltages

* Table (7) presents the measured Power conversion efficiency (Ƞconv), European power conversion efficiency (ȠconvEUR) and Californian power conversion efficiency (ȠconvCEC).

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Ƞconv** | | | | | | | | **(Ƞcov EUR)** | **(Ƞconv**  **CEC)** |
| 5% | 10% | 15% | 25% | 30% | 50% | 75% | 100% |
| **Umpp**  **Min = 390V** | 0.94 | 0.96 | 0.97 | 0.97 | 0.97 | 0.97 | 0.96 | 0.96 | 0.96 | 0.97 |
| **Umpp nom 600V** | 0.96 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 |
| **Umpp max = 800V** | 0.97 | 0.97 | 0.98 | 0.98 | 0.98 | 0.98 | 0.97 | 0.97 | 0.97 | 0.98 |

Table 7: Measured Ƞconv, ȠconvEUR and ȠconvCEC of theDuT

* Over / Under voltage test (IEC/EN 61727 Grid code parameters set on the DuT)
* The response time of the DuT is measured as per the methodology briefed in section 4.2 of this report and compared against the values stipulated in IEC / EN 61727. Table (8) presents the measured results. The measured response time of all the voltage and frequency ranges is observed to be well within the stipulated time frames.

|  |  |  |
| --- | --- | --- |
| **Voltage Range**  **(At PoC)** | **IEC/EN 61727**  **Response time (secs)** | **Measured response time (secs)** |
| V < 50% | 0.1 | 0.086 |
| 50% ≤ V <85% | 2.0 | 1.998 |
| 85% ≤ V ≤ 110% | Continuous operation | Continuous operation |
| 110% < V < 135% | 2.0 | 1.963 |
| V ≥ 135% | 0.05 | 0.053 |
| **Frequency Range** |  |  |
| >49Hz | 0.2 | 0.006 |
| >51Hz | 0.2 | 0.011 |

Table 8: Measured Vs IEC/EN 61727 response time comparision

* The DuT re-connection time is measured post trip during an over / under voltage and frequency scenario. The time taken by DUT to connect back to the grid after the voltage and frequency returned to normalcy is presented in Table (9).

|  |  |
| --- | --- |
| **Trip trigger points** | **Re-connection time post trip** |
| V < 50% | 132.60 |
| 50% ≤ V <85% | 135.71 |
| 110% < V < 135% | 132.04 |
| V ≥ 135% | 135.89 |
| **Frequency Range** |  |
| >49Hz | 134.76 |
| >51Hz | 132.68 |

Table 9: Re-connection time of the DuT post trip

* The real time plots in Figure (12) to (23) presents the measured time in more detail for each of the test case mentioned in Table (8) and (9).

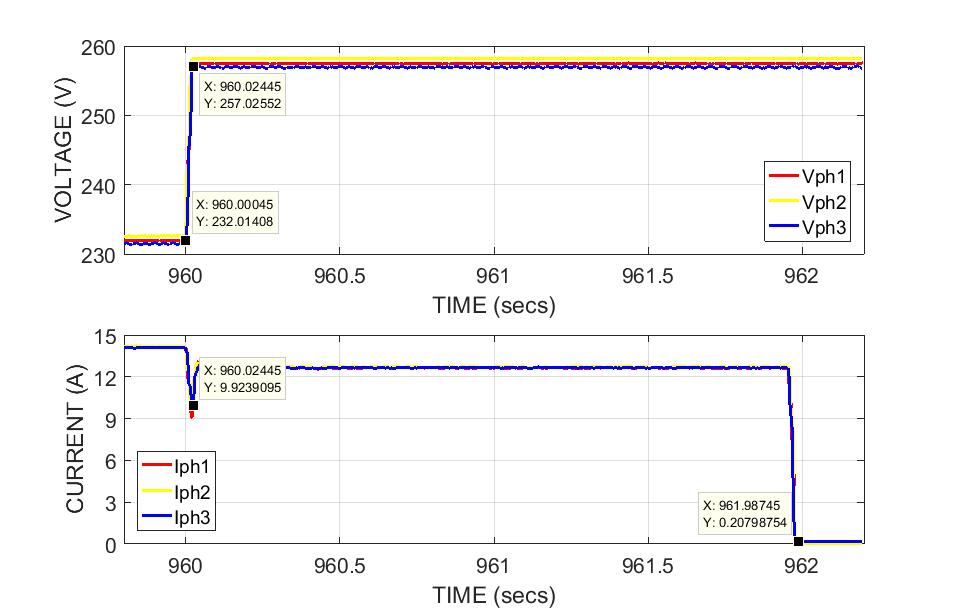


Figure 12: Response time for the over voltage exceeding 110% of the VRMS

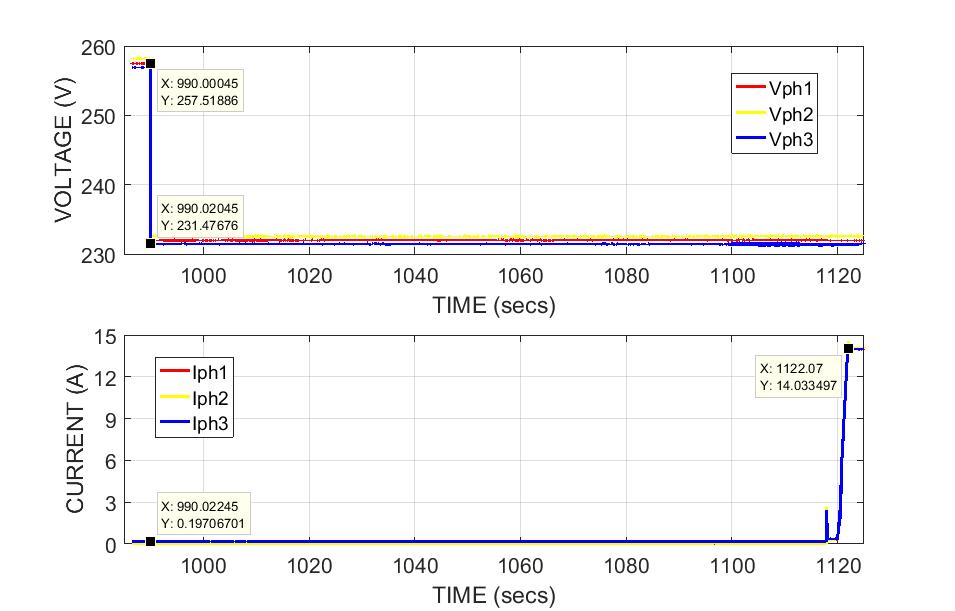


Figure 13: Re-connection time post trip during over voltage exceeding 110% of VRMS

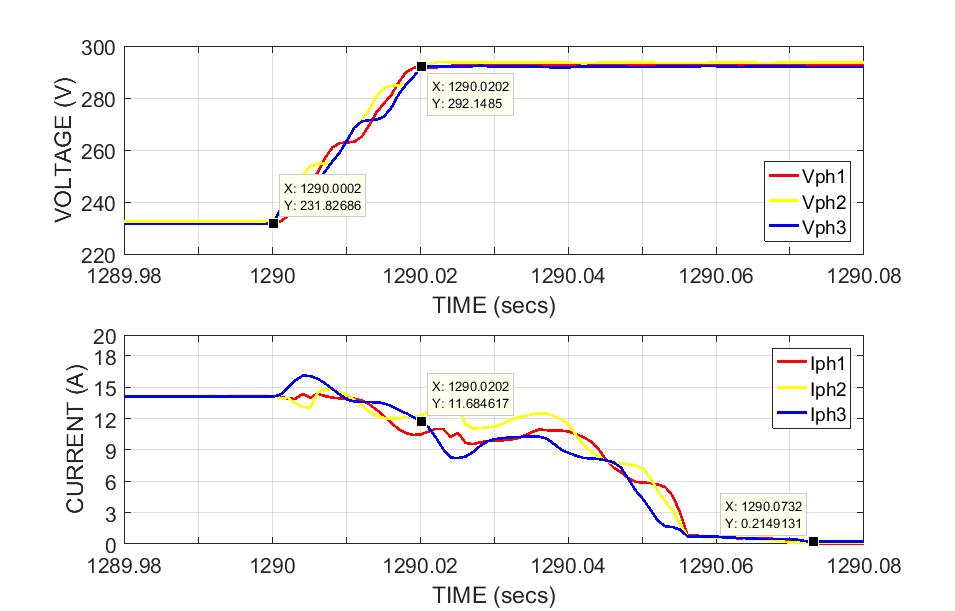


Figure 14: Response time for the over voltage exceeding 135% of the VRMS

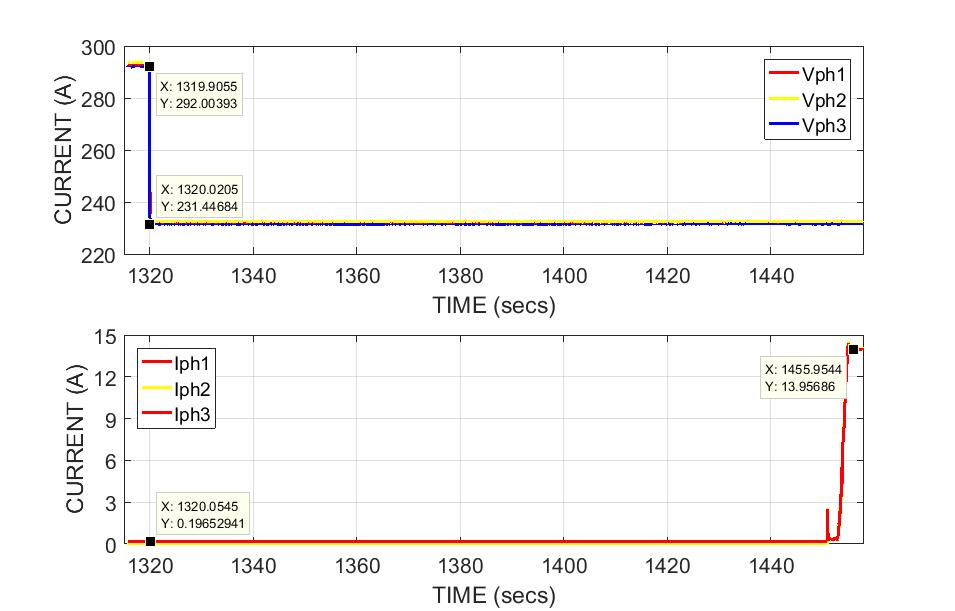


Figure 15: Re-connection time post trip during over voltage exceeding 110% of VRMS

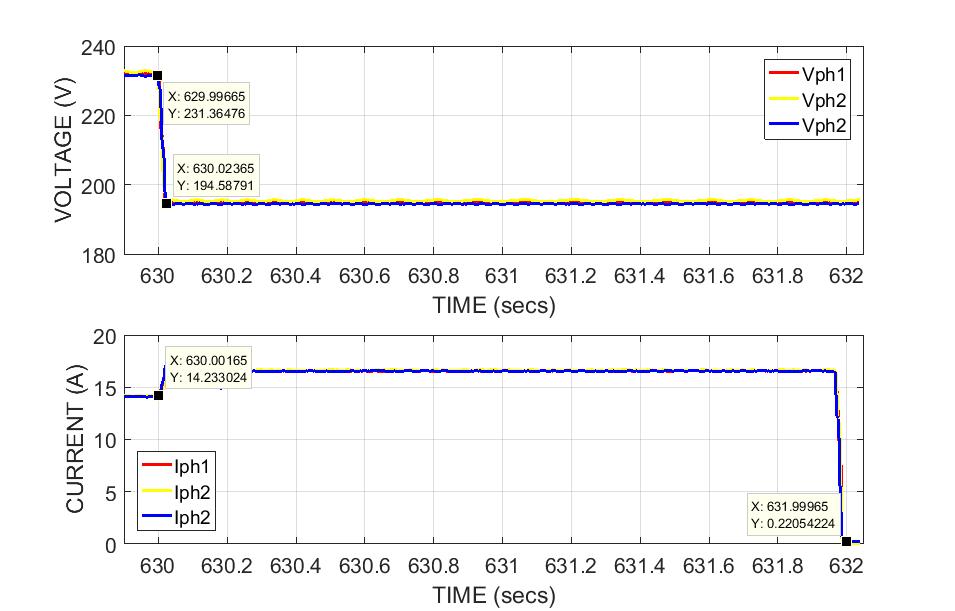


Figure 16: Response time for the under voltage exceeding 85% of VRMS

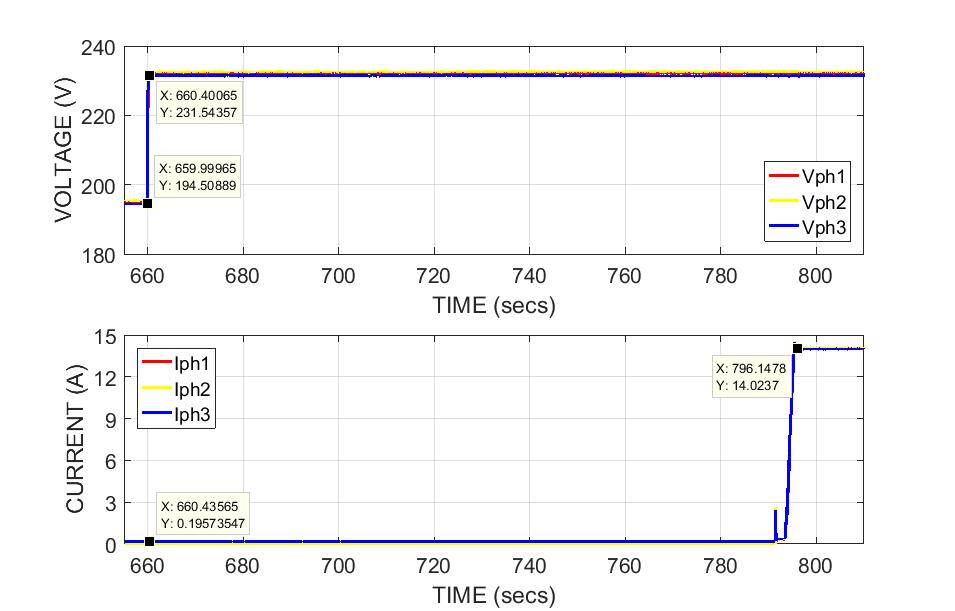


Figure 17: Re-connection time post trip during under voltage exceeding 85% of VRMS

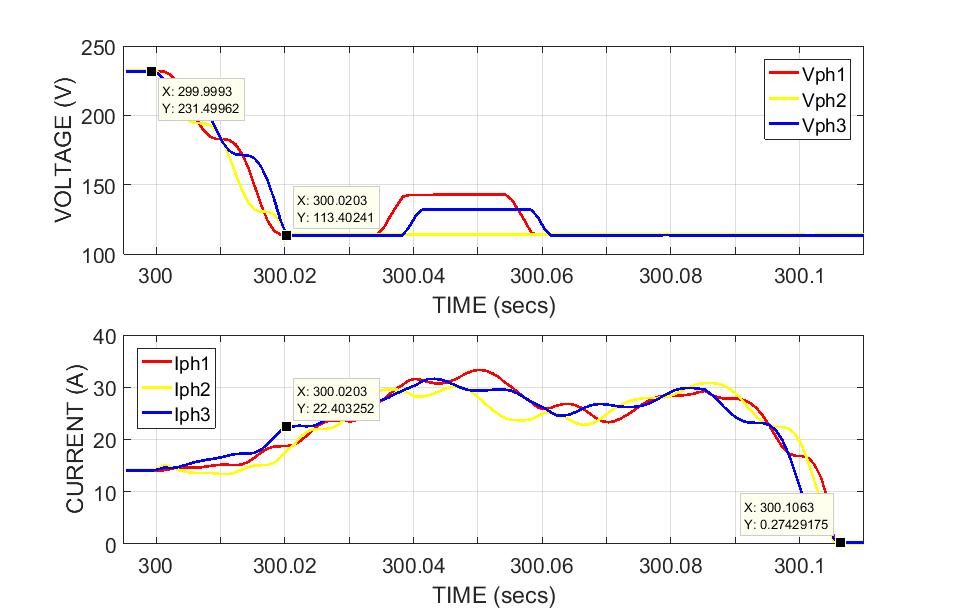


Figure 18: Response time for the under voltage exceeding 50% of the VRMS

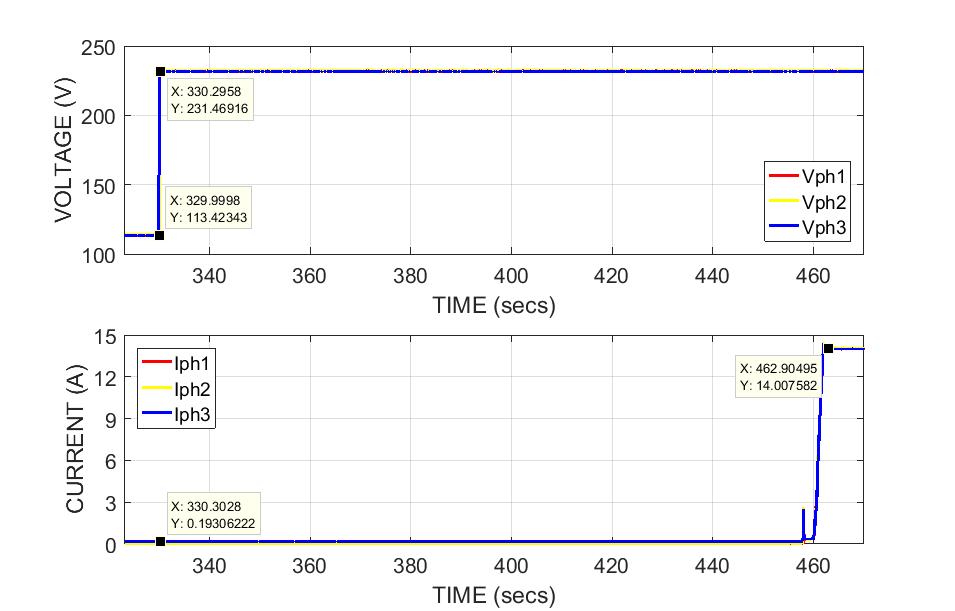


Figure 19: Re-connection time post trip during under voltage exceeding 50% of VRMS

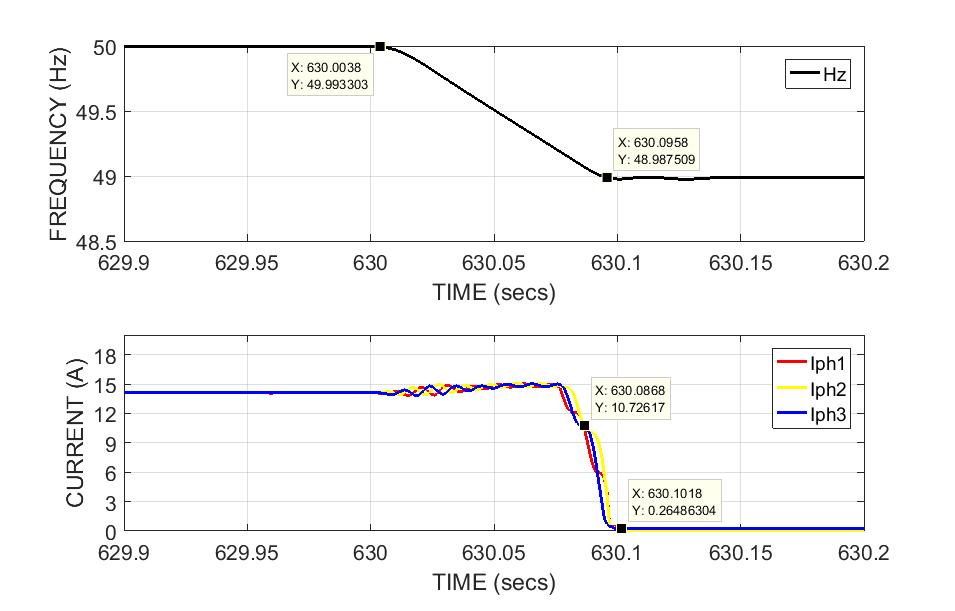


Figure 20: Response time for the under frequency exceeding 49Hz

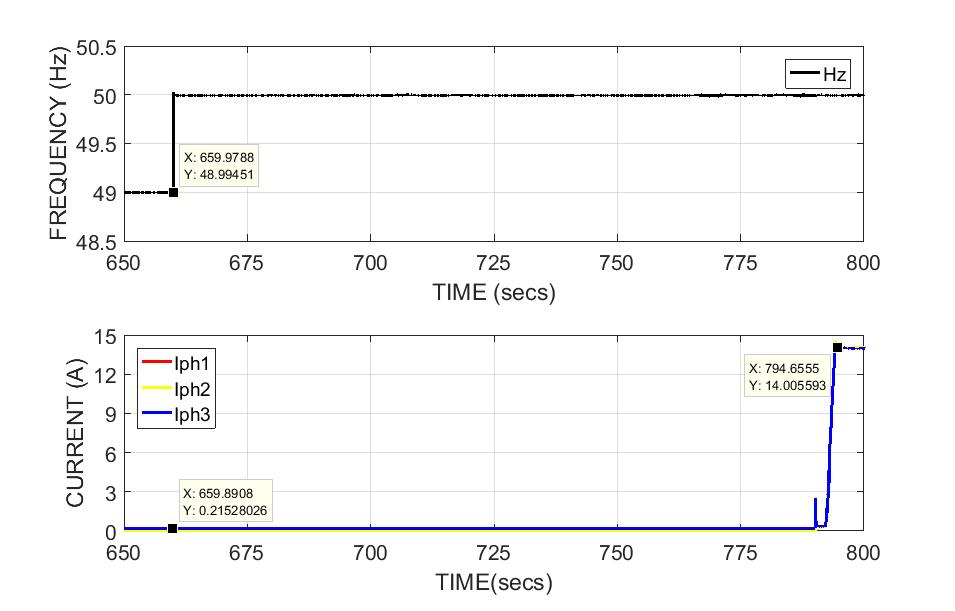


Figure 21: Re-connection time post trip during under frequency exceeding 49Hz

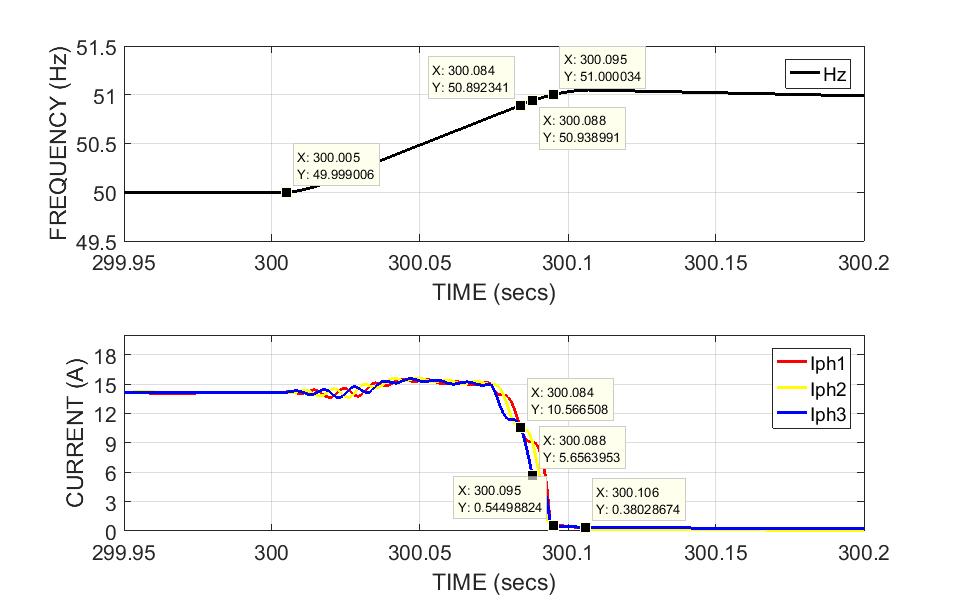


Figure 22: Response time for the over frequency exceeding 51Hz

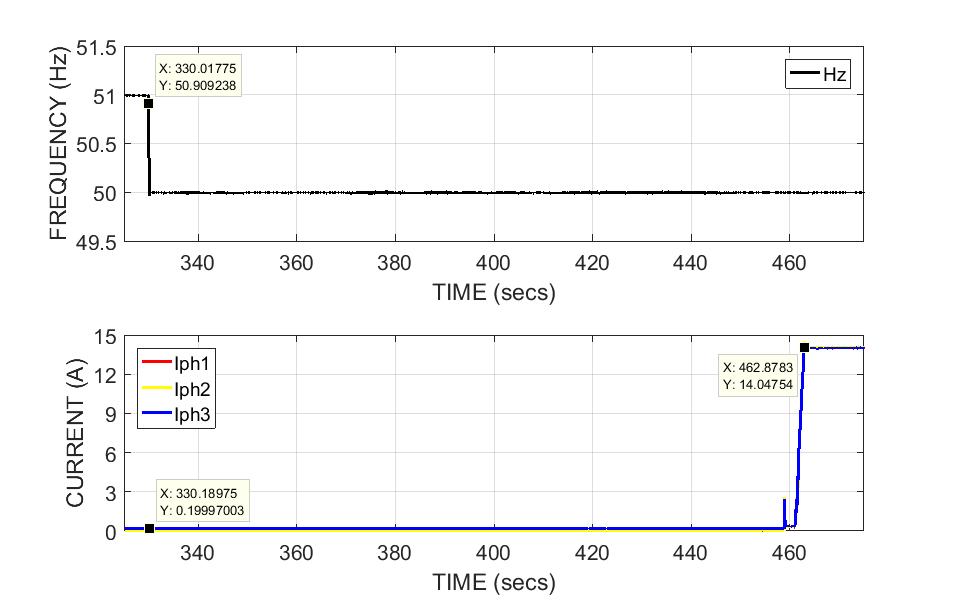


Figure 23: Re-connection time post trip during over frequency exceeding 51Hz

* Over / Under voltage test (Grid code parameters set to Default on the DuT)
* The response time of the DuT is measured as per the methodology briefed in section 4.2 of this report and compared against the values stipulated in NRS097-2-1. Table (8) presents the measured results and it is observed at couple of voltage ranges, the measured results are outside the boundary limits. The measured results raise serious concerns when an installer does not set up the correct grid code applicable to the country and commissions the project with “Default” setting.

|  |  |  |
| --- | --- | --- |
| **Voltage Range**  **(At PoC)** | **Response time (secs)** | **Measured time (secs)** |
| V < 50% | 0.2 | Trips before the voltage level can be taken to 50% |
| 50% ≤ V <85% | 10 | 34.08 |
| 85% ≤ V ≤ 110% | Continuous operation | Continuous operation |
| 110% < V < 115% | 40 | 26.53 |
| 115% ≤ V < 120% | 2 | 0.196 |
| V ≥ 120% | 0.16 | 0.183 |
| **Frequency Range** |  |  |
| <47 Hz | 0.2 | 591.10 |
| 47 ≤ Hz ≤ 50.5 Hz | Continuous operation | Continuous operation |
| 50.5 ≥ Hz ≥ 52 Hz | Active power shall not increase and shall drop at a gradient of 50% per Hz | No increase in power, power drop starts only at 51Hz |
| >52Hz | 0.5 | 0.04 |

Table 10: Measured Vs NRS 097-2-1 response time comparision

* The real time plots in Figure (24) to (34) presents the measured time in more detail for each of the test case mentioned in Table (9).

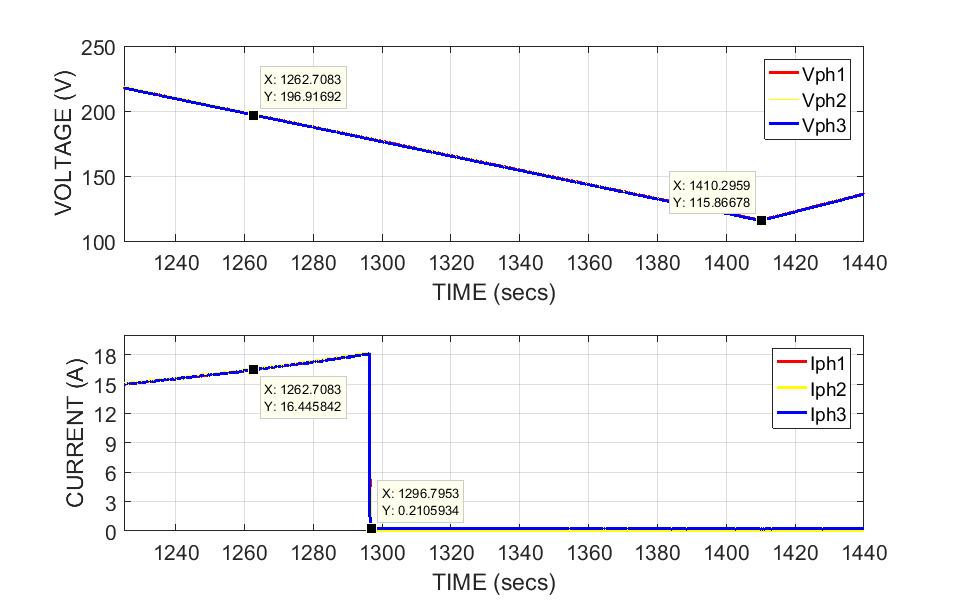


Figure 24: Response time for the under voltage exceeding 85% of the VRMS

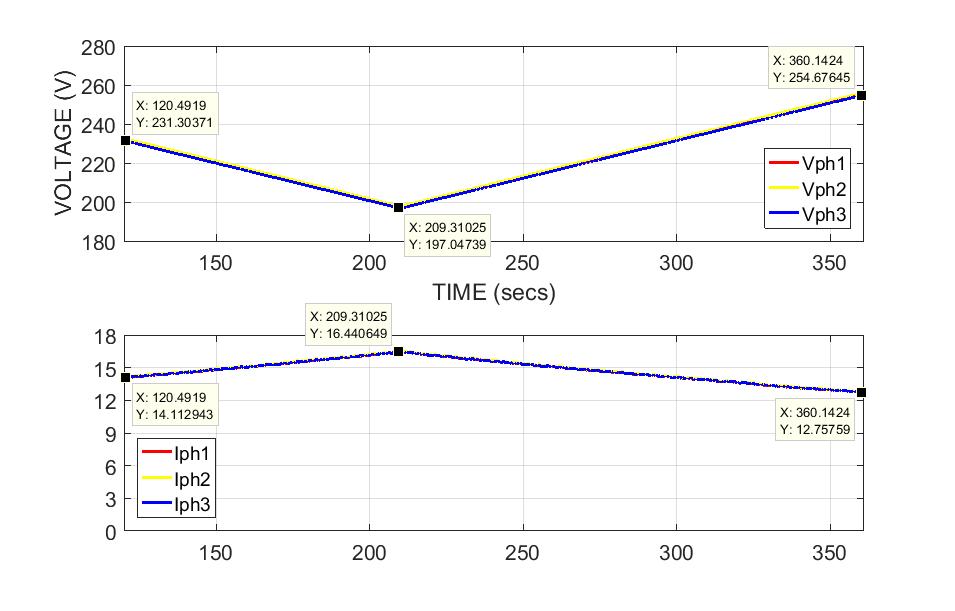


Figure 25: Continuous operation of DuT during above 85% and below 110% of the VRMS



Figure 26: Response time for the over voltage exceeding 110% of the VRMS

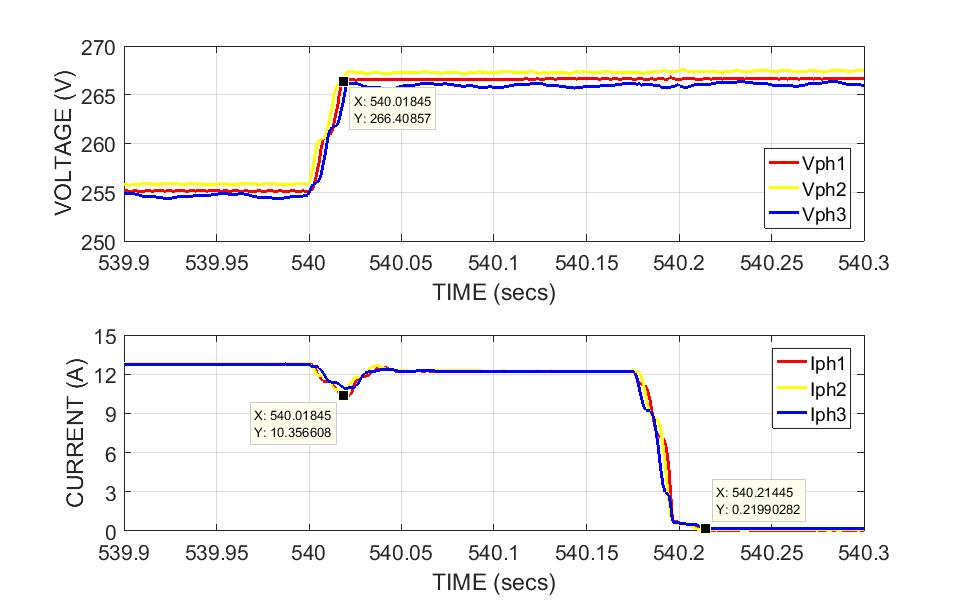


Figure 27: Response time for the over voltage exceeding 115% of the VRMS

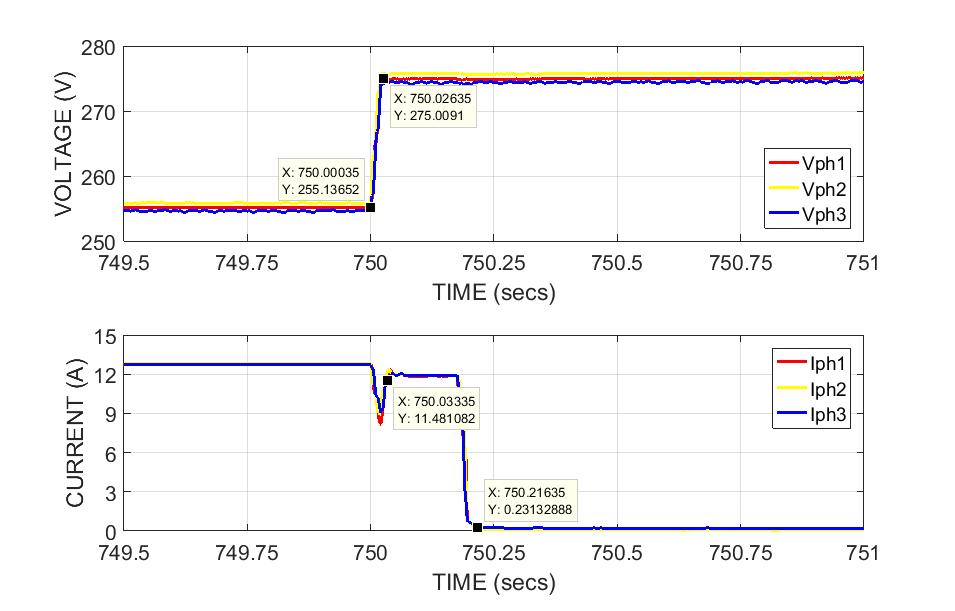


Figure 28: Response time for the over voltage exceeding 120% of the VRMS

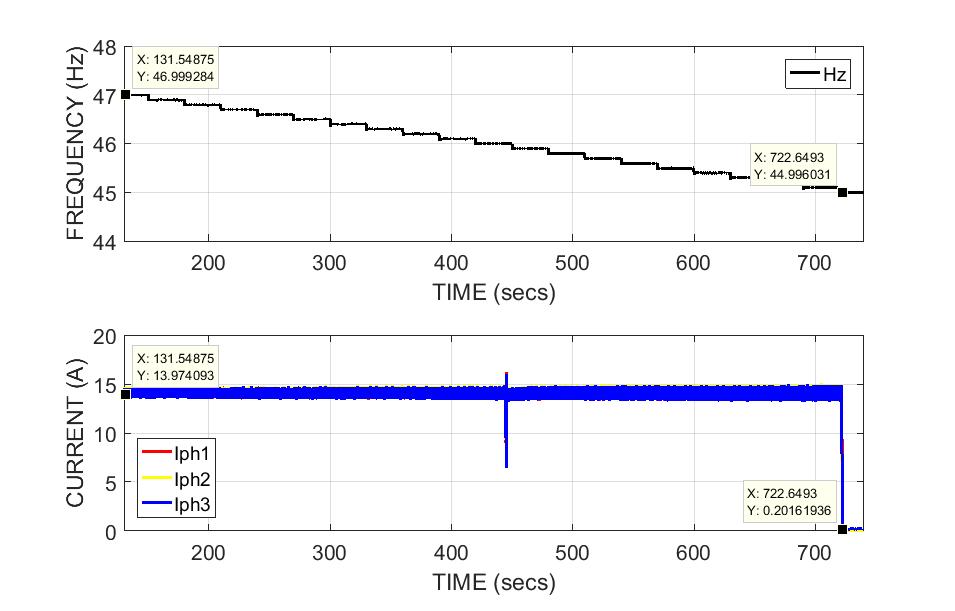


Figure 29: Response time for the under frequency exceeding 47Hz

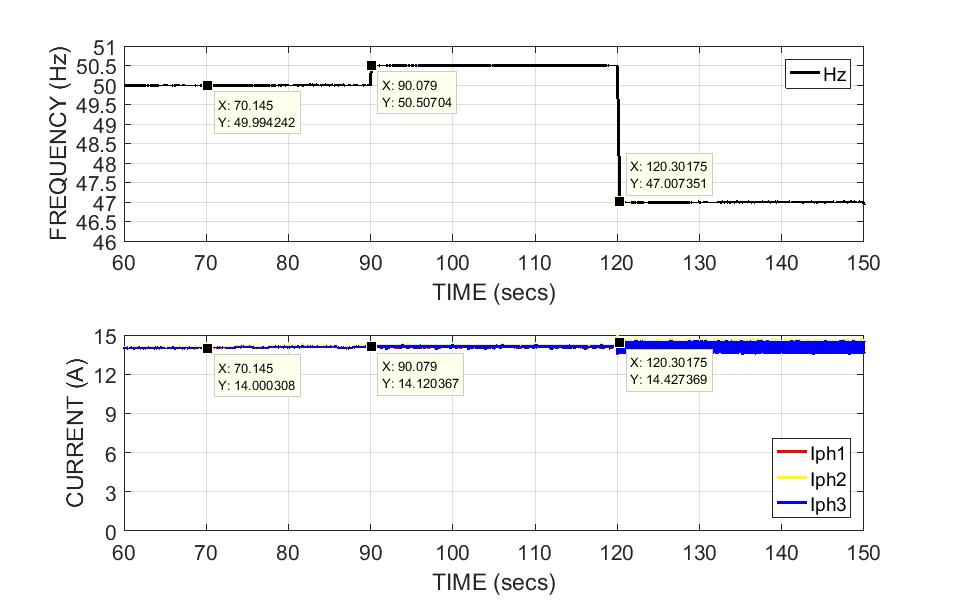


Figure 30: Continuous operation for the frequency 47Hz to 50.5Hz

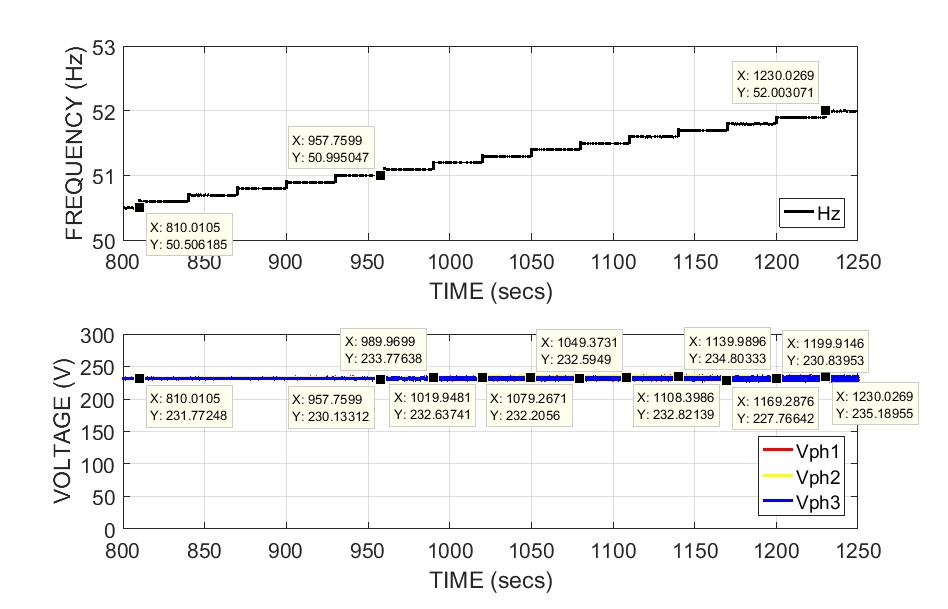


Figure 31: Status of Voltage with increasing frequency from 50.5Hz to 52Hz

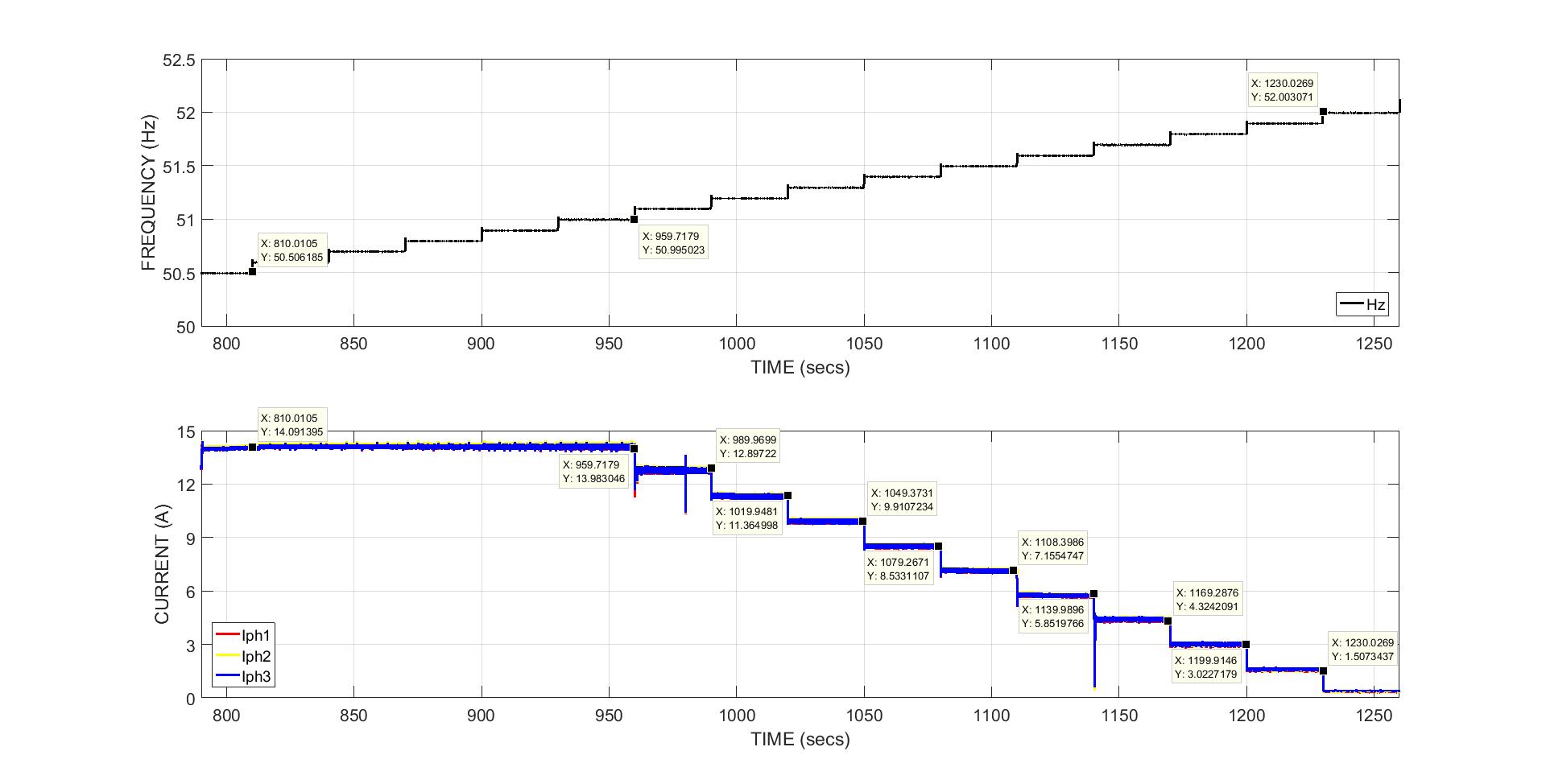


Figure 32: Status of Current with increasing frequency from 50.5Hz to 52Hz

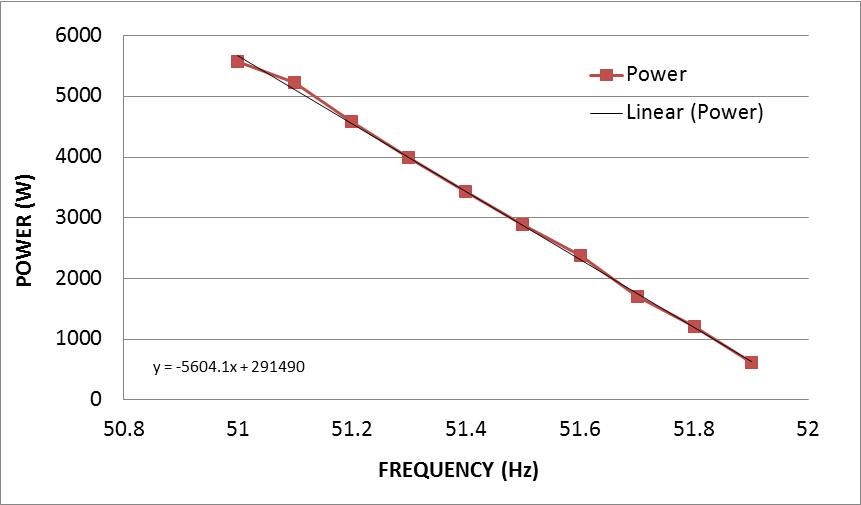


Figure 33: Gradient of power during frequency increase from 50.5 to 52Hz

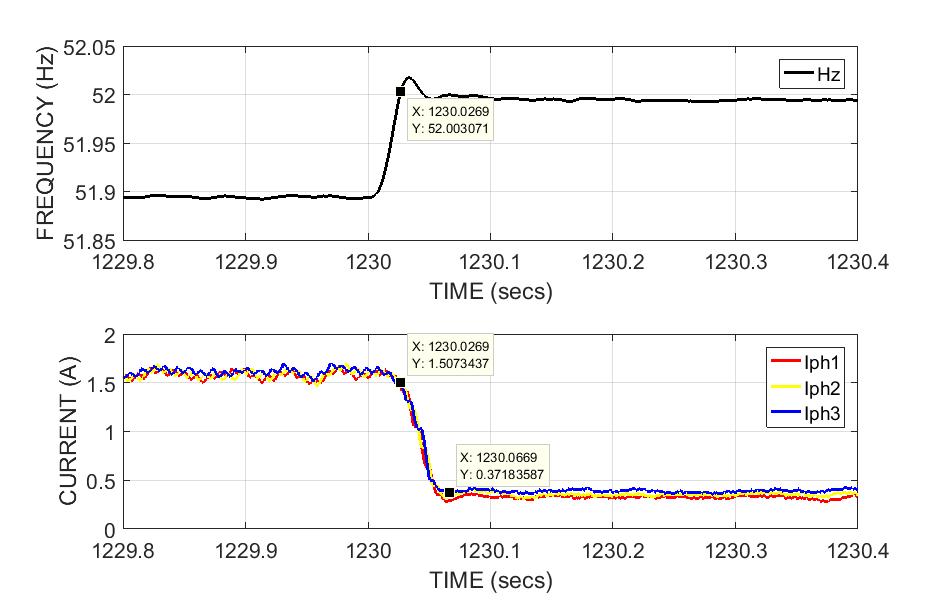


Figure 34: Response time for the under frequency exceeding 52Hz

* Ride through functionality test
* The ride through functionality of the DuT during short term voltage dips is tested as per the methodology briefed in section 4.2. The monitored status for each of the voltage dip is presented in the table (10).

|  |  |  |  |
| --- | --- | --- | --- |
| **Dip type** | **Ride through voltage levels** | **Duration** | **Monitored status** |
| Y type | 10% ≤ V ≤ 15% | 2000 ms | Ride through |
| Y type | 15% ≤ V ≤ 20% | 600 ms | Ride through |
| Y type | 20% ≤ V ≤ 30% | 150 ms | Ride through |
| X1 type | 30% ≤ V ≤ 40% | 150 ms | Ride through |

Table 11: Monitored Vs IEC/EN 61727 requirement

* The real time plots in Figure (35) to (38) presents the ride through functioning by DuT for the duration specified during different voltage levels as mentioned in Table (10).

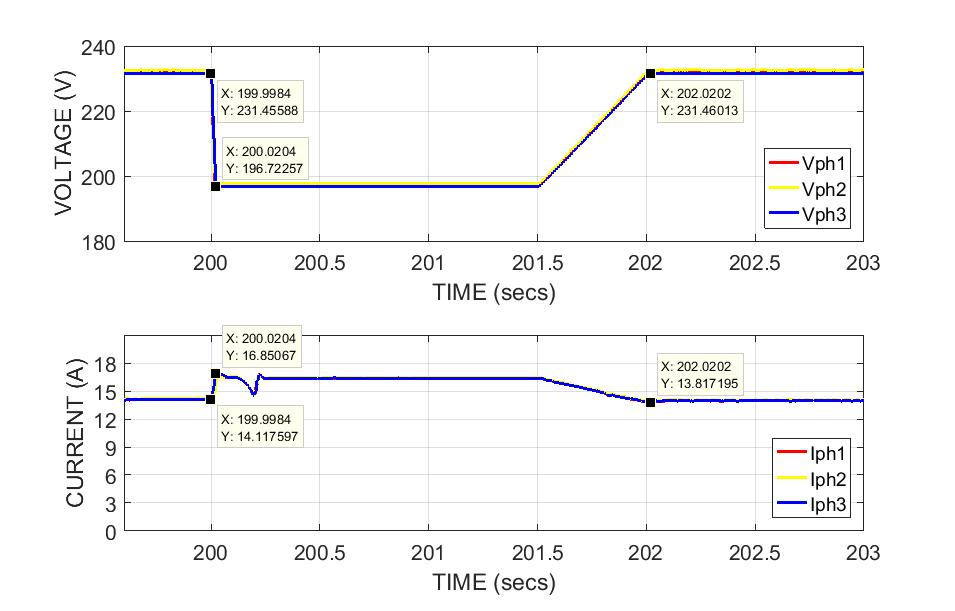


Figure 35: DuT ride through functionality during 15% voltage dip for 2000mS

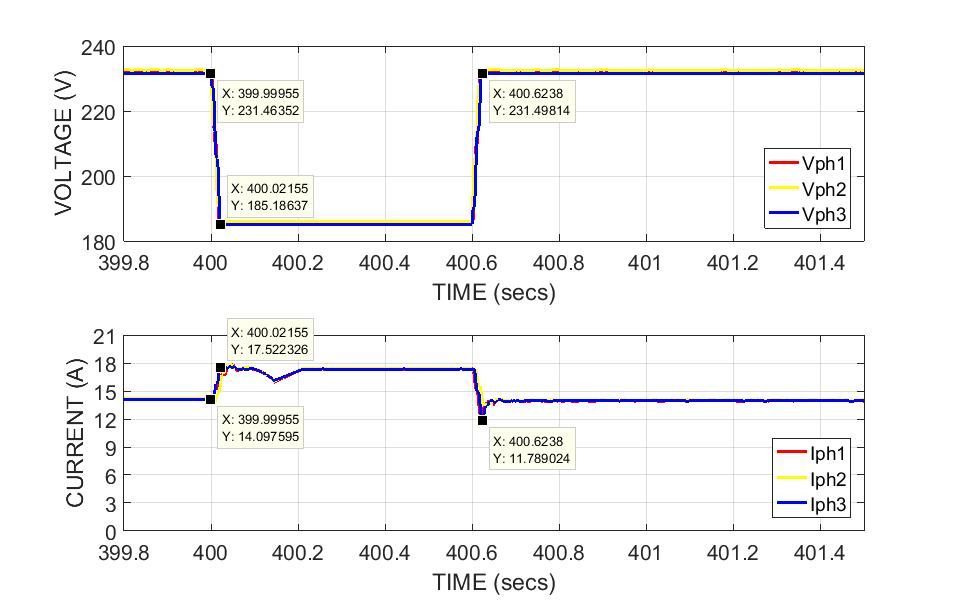


Figure 36: DuT ride through functionality during 20% voltage dip for 600mS

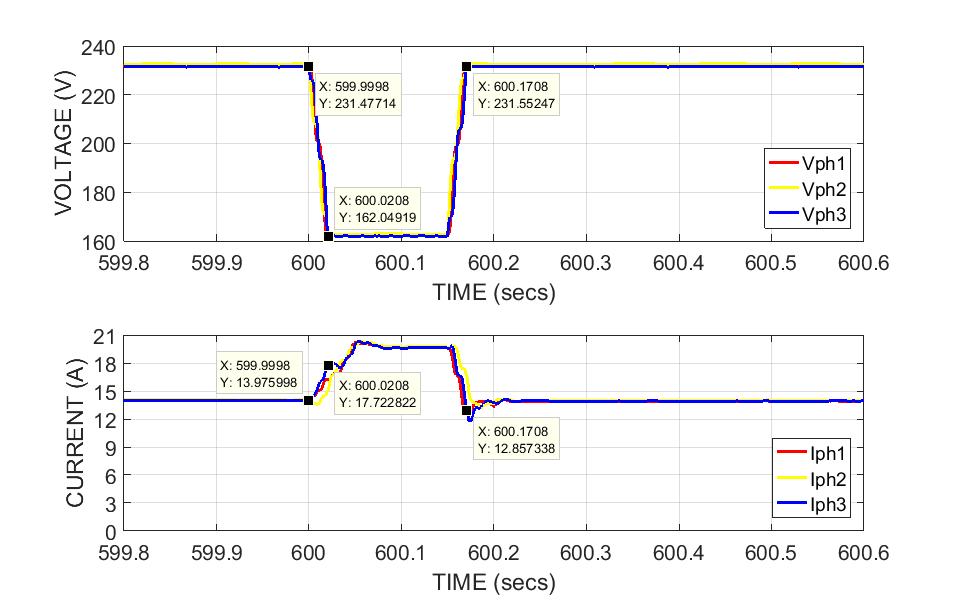


Figure 37: DuT ride through functionality during 30% voltage dip for 150mS

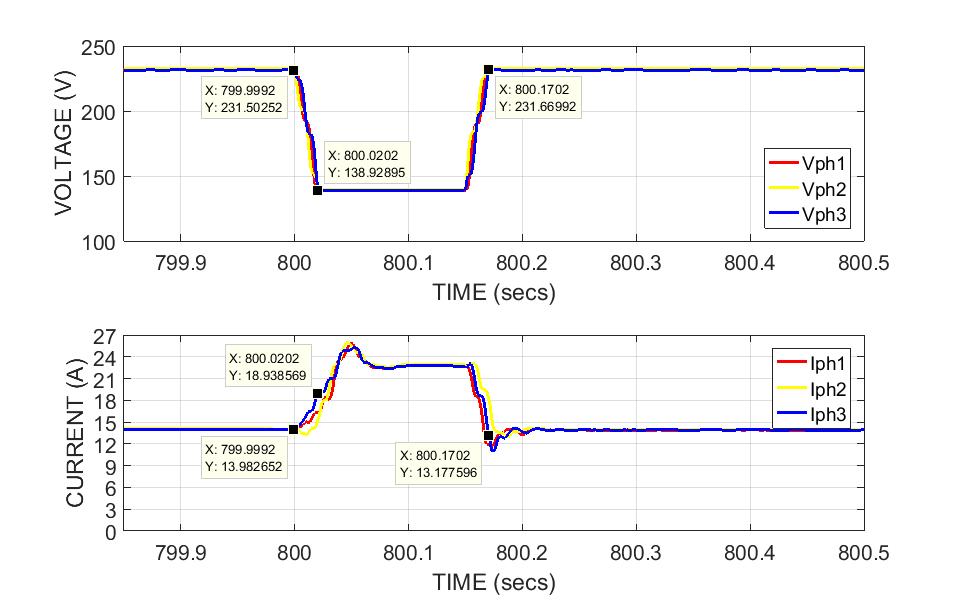


Figure 38: DuT ride through functionality during 40% voltage dip for 150mS

* Harmonic measurements:
* The total harmonic distortions measurement is carried out as per the steps briefed in section 4.2. The measured fundamental AC current (I ph) for all the 3 phases is plotted against the solar irradiance profile and is presented in Figure (38).
* A good overlay of the generation profile of current over irradiance indicate there are no outliers in the measurement and the harmonics outcome can be co-related to irradiance conditions or turn ON of OFF periods.
* Figures (40) to (46) presents the measured THD, Odd harmonic distortions for orders 3rd to 9th, 11th to 15th, 17 to 21st and 23rd to 33rd, Even harmonics distortions for orders 2nd to 8th and 10th to 32rd for all the 3 phases for a clear and cloudy sky irradiance profiles.
* A high THD in all 3 phases is observed for both the sky conditions during early and late sun hours of the day i.e. period when an inverter tends to turn ON with increasing irradiance and tending to turn OFF when the irradiance levels are dipping sharply at the end of the day.
* The measured THD is well above the requirement of 5% in the EN61727 standard.
* The THD measured for a cloudy day profile is also higher than the clear day and crosses the maximum limit of 5%.
* Similar results are observed for the rest of the odd orders from 3rd to 9th, 11th to 15th, 17th to 21st and 23rd to 33rd and even orders of 2nd to 8th and 10th to 32rd.
* It is also observed that some of the harmonics in the network is absorbed by the filters in the inverter during the course of the day or peak power generations.

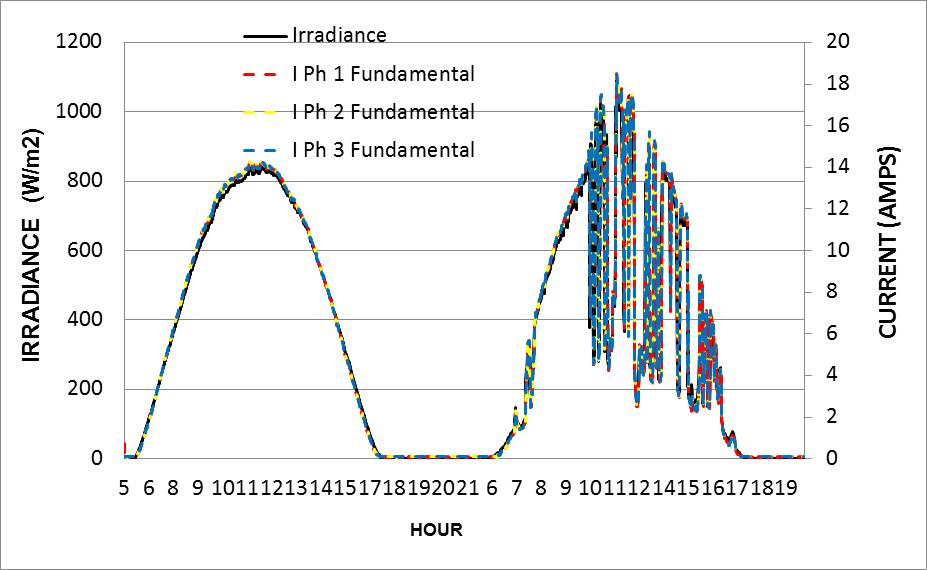


Figure 39: Overlay of measured fundamental current for 3 phases over clear and cloudy irradiance profiles

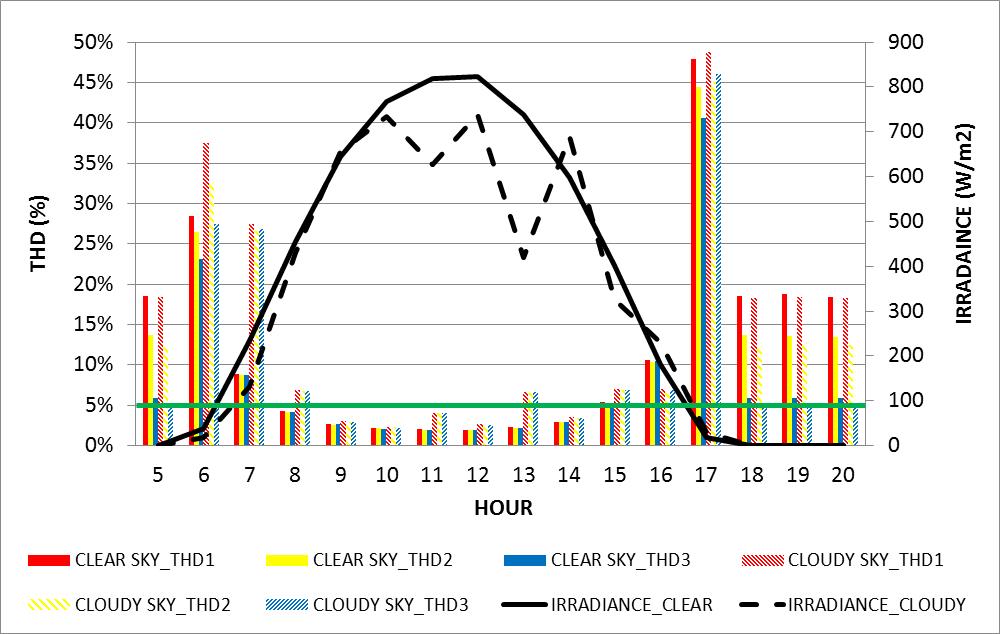


Figure 40: THD measured for clear and cloudy day irradiance profile



Figure 41: Harmonic distortions measured for the odd orders from 3rd to 9th

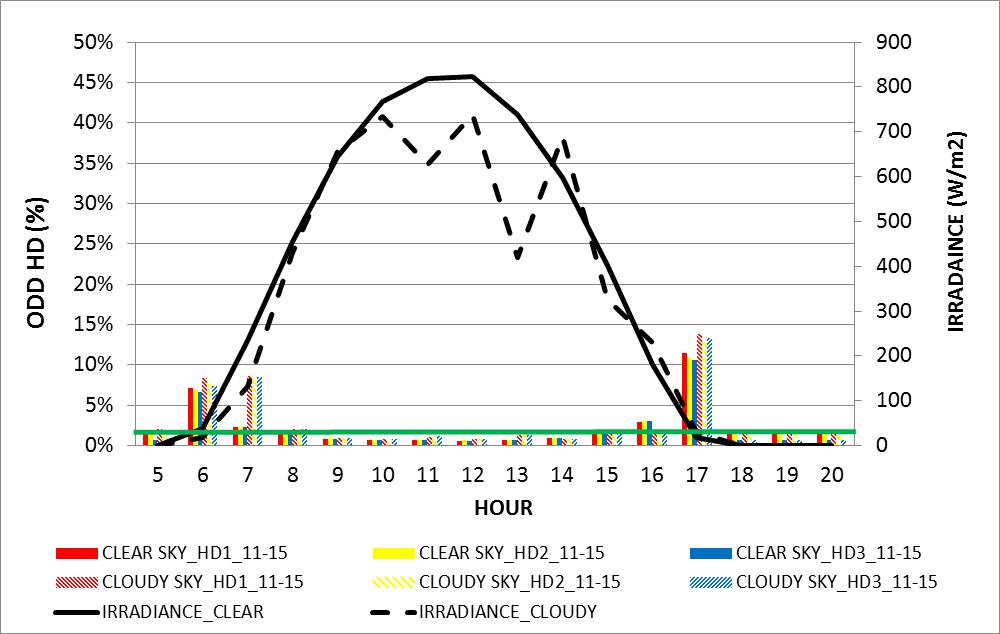


Figure 42: Harmonic distortions measured for the odd orders from 11th to 15th

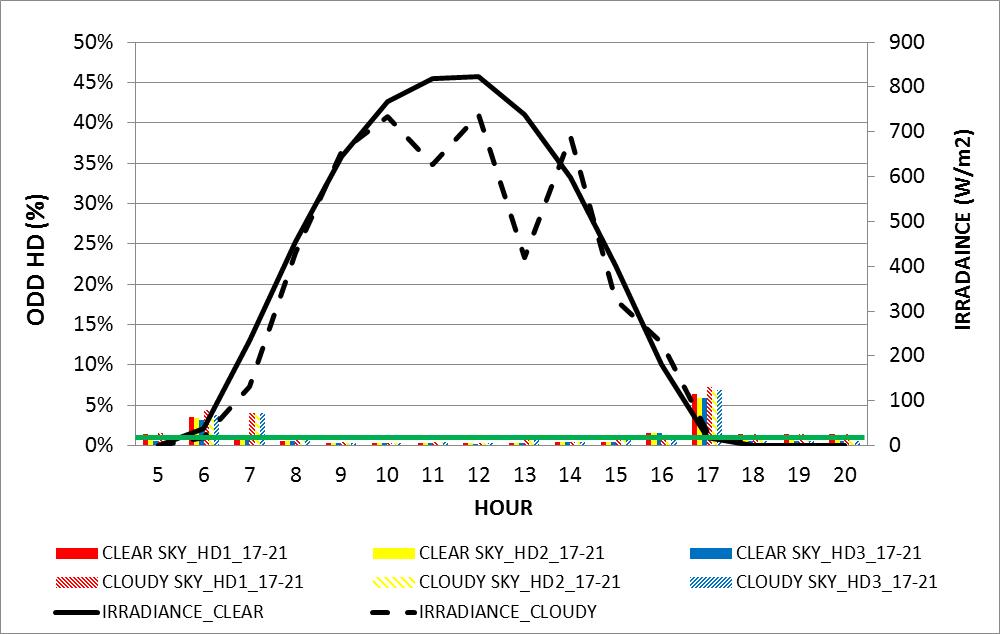


Figure 43: Harmonic distortions measured for the odd orders from 17th to 21st

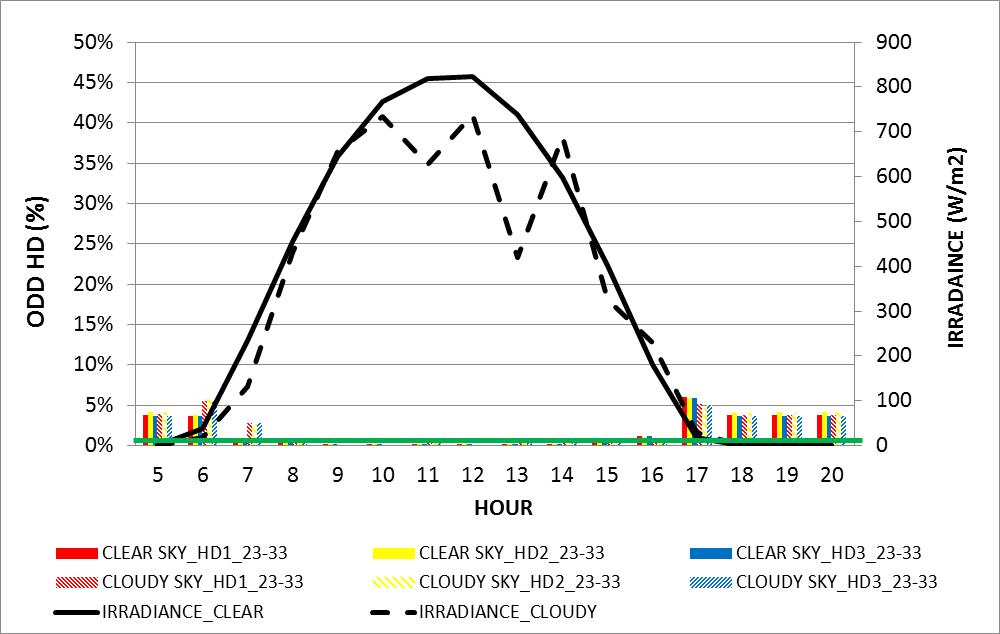


Figure 44: Harmonic distortions measured for the odd orders from 23rd to 33rd

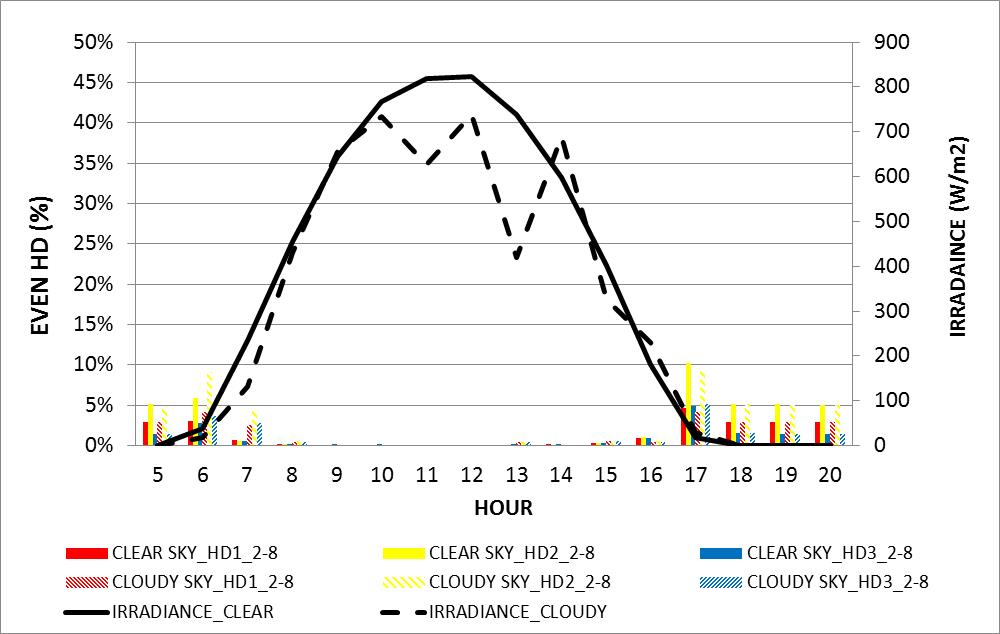


Figure 45: Harmonic distortions measured for the even orders from 2nd to 8th



Figure 46: Harmonic distortions measured for the odd orders from 10th to 32nd

* Islanding test:
* An attempt is made to verify the anti-islanding functionality of the solar inverter when the active power of generation to load ratio is -5% and the reactive power is at +5%.
* It is noted during the exercise that the test is repeated for many combinations of active and reactive power as briefed in section 4.2.
* It is also understood that to reach the active and reactive power to the specified ratios as per the standard consumes more time and a precise and sophisticated test infrastructure to carry out the islanding test.
* Figure (47) presents the status of voltage, current, active and reactive power during the test. The active power in the network is balanced to -5.6% and due to time limitations, reactive power could not be balanced to 5% as per the standard requirement.
* Figure (48) presents the measured trip time after the loss of grid when the active power of generation to load is at -5%.
* The time taken by the inverter to check the loss of the grid and stop supplying the power to the closely matched demand by the loads is 0.108secs which is well within the limit of 2s specified in IEC/EN standard 62116.
* It is noted that it is a learning activity and further efforts will be made in the future to balance the active and reactive power as per Table (6) and repeat the tests to determine more meaningful test results.

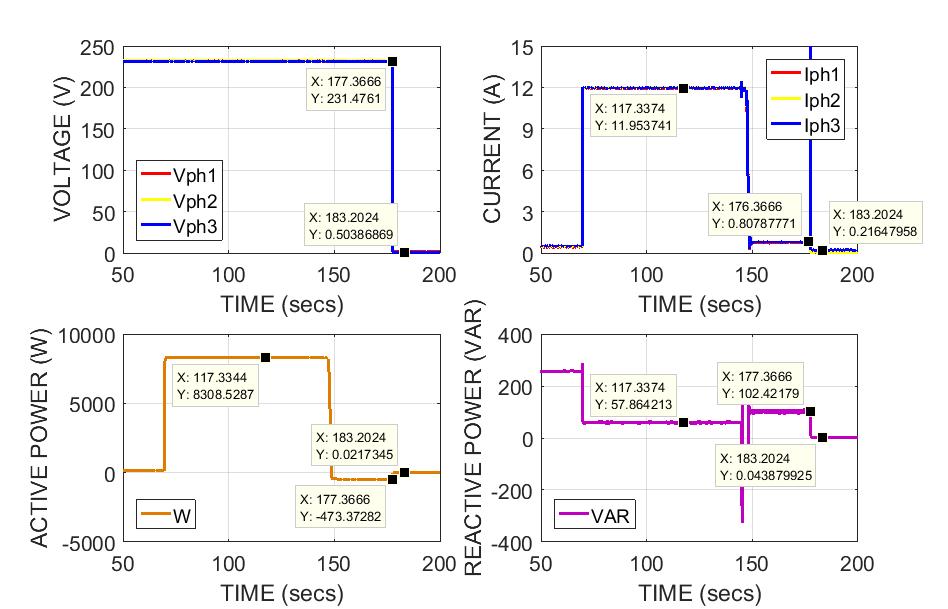


Figure 47: Measured voltage, current, active and reactive power during islanding test

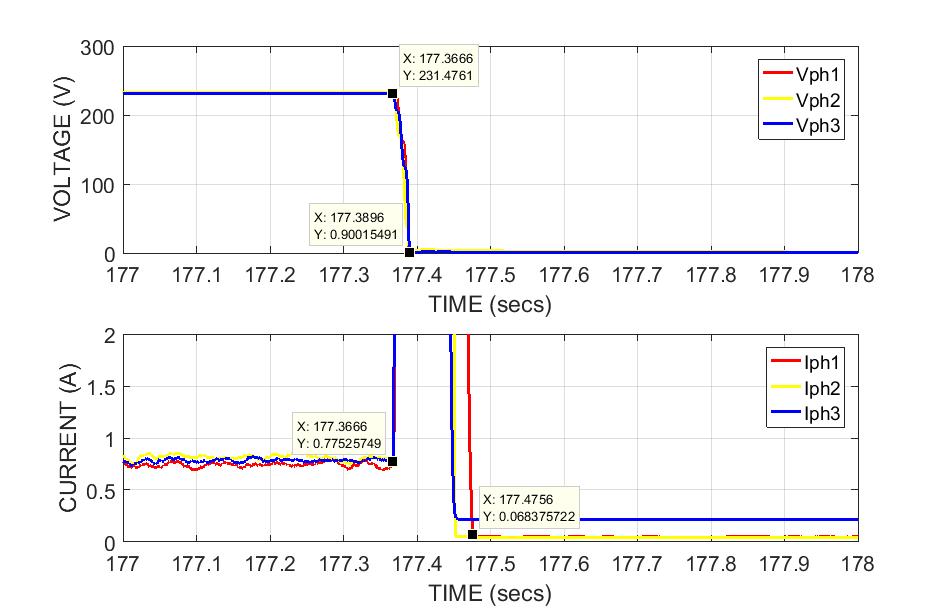


Figure 48: Response time of DuT during islanded condition

# Open Issues and Suggestions for Improvements

Within the given provisions and allocated time under this program, a lot of effort has been put to understand, set-up, monitor, measure, analyse and conclude few of the inverter characterization tests. There is plenty of room for the improvements and incorporate the lessons learnt at our proposed laboratory in the near future and serve the local solar PV industry. It is a worthwhile experience before we venture out and establish infrastructure for the inverter characterization, of-course depending on how quickly we secure funding’s for this project.

# Dissemination Planning

The exposure to real time inverter characterization at CEA-INES laboratory has certainly enhanced our know how on the configurations and protection system within the inverter, test infrastructure, test procedures, deep dive into the protocols per standards, real time measurements and validation of test results. The experience will position us to establish our own inverter characterization facility above our existing solar PV module and battery storage characterization facilities within the institution.

The results obtained during this program will be published at one of the conferences or workshops scheduled within the country during the calendar year 2020. The experience gained during this program will be disseminated to colleagues, students and other interested parties during our scheduled monthly meetings or brown-bag sessions.

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[5] IEC/EN 62116: Utility-interconnected photovoltaic inverters – Test procedure of islanding prevention measures

[6] EN50530: Overall efficiency of grid connected photovoltaic inverters

[7] NRS097-2-1: Grid interconnection of embedded generation Part 2: Small scale embedded generation Section 1: Utility interface

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