# TRANSNATIONAL ACCESS

# USER PROJECT FACT SHEET

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| **USER PROJECT** |  |
| **Acronym** | **Solar photovoltaic (PV) Inverter characterization and power quality analysis** | |
| **Title** | **Inverter characterization, determine efficiency, conformance checks and measure harmonic distortions of a solar PV inverter connected to controlled loads at CEA, France** | |
| **ERIGrid Reference** | **654113 - INFRAIA-1-2014/2015: Integrating and opening existing national and regional research infrastructures of European interest** | |
| **TA Call No.** | **5th** | |

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| **HOST RESEARCH INFRASTRUCTURE** | |  | | | |
| **Name** | **Centre for Nuclear Energy and Alternative Energies (CEA), INES, 17 Avenue Des Martyrs, Grenoble 38054** | | | |
| **Country** | **France** | | | |
| **Start date** | **02 Sep 2019** | | **Nº of Access days** | **22** |
| **End date** | **01 Oct 2019** | | **Nº of Stay days** | **28** |

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| **USER GROUP** |  |
| **Name (Leader)** | **Manjunath Basappa Ayanna** |
| **Organization (Leader)** | **Council for Scientific and Industrial Research (CSIR)** |
| **Country (Leader)** | **South Africa** |
| Name | **NA** |
| Organization | **NA** |
| Country | **NA** |

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| 1. **USER PROJECT SUMMARY** (objectives, set-up, methodology, approach, motivation) |
| **Objective:**  Due to significant drop in PV prices, many consumers are switching to embedded generation to reduce the ever increasing electricity tariffs in the country. South African utility company has raised concerns about the un-safe inverter operations during low voltage grid network maintainace periods. Also there are concerns of increased injection of harmonic levels due to high frequency switching devices (inverters) coming in-line into the low voltage grid network. The objective of this project is to mainly increase our know-how and capability in the field of inverter characterization within the country and further carry out detailed research on power quality issues with embedded generation.  **Scope:**  Characterize a solar inverter to determine efficiency, perform anti-islanding tests, measure the inverter response time during over / under voltage frequency situations and measure harmonic distortions of a solar PV inverter connected to controlled load and gird conditions at solar PV laboratory, CEA-INES, Le Bourget Du Lac, France  **Motivation:**  Grid-tied PV systems are the fastest growing renewable energy source for power generation today. The quality of the electricity produced from PV directly depends on the amount of solar irradiance. Changes in weather conditions, rainfall and cloud movements affect the output power from PV. The primary reason for variable output power from PV is due to cloud movements. These power fluctuations on a grid-tied low voltage network also causes harmonic distortions in current waveforms [1]. PV inverters are the main source of injecting current harmonics into the network. The injected harmonics can increase power losses in the system [2]. There’s a motivation worldwide to conduct power quality analysis as more embedded generators particularly solar PV systems are connected to low voltage utility grid. High penetration of intermittent PV cause voltage fluctuations in grid, voltage rise and reverse power flow, power fluctuations in grid, variation in frequency and grounding issues. PV penetration in low voltage distribution network also causes harmonic distortion in current and voltage waveforms [3]. Power quality analysis includes harmonic distortions, reverse power flow, voltage fluctuations and power fluctuations. These parameters must comply with the governing standards in order to ensure the safe operation of connected loads and cleanliness of the supply. In South Africa, the solar PV modules characterization is carried out only at CSIR EC, Pretoria and Nelson Mandela University, Port Elizabeth. CSIR EC houses the country’s first solar PV reliability test lab which includes climatic chambers, sun simulator, mechanical load tester, outdoor IV characterization systems etc. We have already ear-marked space in our existing solar PV reliability laboratory for developing solar PV inverter test infrastructure and support the local PV industry.  The proposed inverter test facility at our premises will be a research platform for many students to carry out research on locally developed power converters. Under the ERIGrid TA access program, we aimed to expand our knowledge base and capability in the field of inverter characterization and establish test and research facility in the country. Furthermore, the confidence of customers and the general public into the PV technology could be strengthened by supplying locally compiled test data and results.  We foresee the below potential benefits from our solar PV testing facility (mainly PV modules and inverters):   * Developing competencies in the development of solar energy technologies * Training & development of the necessary manpower to design, construct, operate and maintain PV power plants * In-country training of personnel for renewable energy projects : Engineers, in collaboration with Universities, Technicians and technologists, in collaboration with Universities of Technology, Specialist artisans, in collaboration with Further Education and Training (FET) colleges * To contribute in the development of a new generation of trained scientists at PhD, Masters and Honours levels   The establishment of the test facility at the CSIR would mean that new technologies can be tested locally instead of sending them to other facilities overseas. This would have the advantage of:   * Elimination of the requirement for international travel, which results in greatly reduced transport costs and the ability to utilize or train larger numbers of people for longer periods of time for an existing budget * Shorter lead times for travel, as personnel do not require visas and equipment does not have to pass through customs * The ability to expose non-specialists such as decision-makers, journalists and schoolchildren to in-country developments * It will allow for greater flexibility by not being reliant upon testing schedules at foreign facilities * The facility will provide the freedom to pursue work in the South African interest, without being constrained by the interests or capabilities of foreign institutions' staff or facilities   The successful completion of technical exposure at CEA-INES under ERIGrid TA program will enable us to develop our skills in inverter characterization domain. This also enhances our capability in the country to establish and provide end to end testing solutions for all the local manufacturers. The test facility will be a platform for all the research students in the country. The subjection of inverter to controlled load conditions and analyzing the power quality parameters will be a new experience and forms a platform for future research in the organization.  **Executed Tests and Experiments:**  The following tests are carried out in conjunctions with the proposal document on a widely available commercial 3ph 25kWp inverter in the market. The tests are carried out only to get hands on experience in the field of inverter characterization and the results obtained in this study are only for learning purpose and does not certify any product operations.   * Determination of Power conversion efficiency (European and California efficiency) * Determination of trip time of an inverter during over / under voltage situations (Default and EN 61646 grid code settings) * Determination of trip time of an inverter during over / under frequency situations (Default and EN 61646 grid code settings) * Check Inverter ride through functionality during under voltage situations for very short durations * Determine Total Harmonic Distortions (THDi) for the current for a clear and cloudy day irradiance profile * Inverter response time during islanding conditions (Generation to load ratio at -5% and + 5% in active and reactive power respectively)   **Approach:**  The following test plan is derived to execute the earlier mentioned tests. Prior to my arrival at the CEA-INES facility, it is pre-agreed between both the parties to use the available inverter and other lab equipments at the CEA-INES. No test components or measuring equipments are carried from CSIR.   * The scope and type of tests to be carried out at CEA-INES is determined from the ERI Grid project proposal document. * It is decided that all the major operations or infrastructure establishments for the tests to be carried out will be done by CEA personnel as per the organisation policy. * The required skills to carry out the tests are assessed and the availability of the personnel during the project period is assessed. Planning in advance is carried out to keep the tests running during the absence periods of the respective lab personnel.   + Mr. Van Hoa Nguyen is the mentor/supervisor during the course of the project.   + Mr. Marc Jung is assigned as laboratory technician to perform all the electrical infrastructure assembling and interconnection of components.   + I am responsible to determine the type of test, conceptualize, draft test conditions, run the tests, data retrieval, analyse, calculate and compare the measured results against the requirements stipulated in standards. * The environment conditions such as maintaining the required laboratory temperature and barricading the test space to prevent un-authorized entry is done. * Safety induction training is provided to me prior granting the access to the laboratory. * The monitoring parameters for each of the test are identified from IEC/EN 61727, IEC 62116 and EN 50530. * A test schedule is planned for all the working days during my 4 weeks stay period at the facility. Sufficient time is allocated to organise the required equipments and prepare the test infrastructure for each of the test. Table 1 presents weekly schedule to run the planned tests at the the base station and complete reports post return to CSIR.  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | |  | Wk 1 | Wk 2 | Wk 3 | Wk 4 | Wk 5 | Wk 6 | | Power Conversion Efficiency test |  |  |  |  |  |  | | Over / Under voltage tests |  |  |  |  |  |  | | Over / Under frequency tests |  |  |  |  |  |  | | Ride through functionality tests |  |  |  |  |  |  | | Harmonic measurements tests |  |  |  |  |  |  | | Islanding tests |  |  |  |  |  |  | | Data analysis |  |  |  |  |  |  | | Report generation |  |  |  |  |  |  |   Table 1: Inverter characterization test schedule   * Method of the communications during the project is planned and decided mostly to be a verbal communications and always working together with Mr. Van Hoa Nguyen and Mr. Marc Jung. Email interactions whenever required.   **Test set up:**  The following equipments are used to perform the mentioned tests in section 4:   * DC power supply Elektro Automatic PSI 91500-30 * 400V 3 ph+N Grid simulator * Solar inverter - Device under Test (DUT) * Electronic Load (RLC) * Power Analyzer   The below single line diagrams presents the equipments including DuT used to carry out the proposed tests in this project.   * Efficiency test, Over / Under voltage and frequency, Ride through test setup     Figure 1: Single line diagram for efficiency test, over / under voltage and frequency and ride through test   * Harmonic measurements test set up     Figure 2: Single line diagram for Harmonic measurements   * Anti-Islanding test set     Figure 3: Single line diagram for anti-islanding test  **Methodology:**  During proposal phase, it was mentioned that inverters would be tested against South African NRS097 standard. As the Device under Test (DuT) is a commercially available product in France and as the technical exposure under this project is to understand the technicalities involved during inverter characterization, IEC/EN 50530 and IEC/EN 61727 standards are widely used to determine the test sequence, criterions and evaluate the measured results.   * Power Conversion Efficiency test:   + Note the Umppmin, Umppnom and Umppmax voltage of the DuT from rating label.   + For each Maximum Power point Tracking (MPPT) voltage level, power conversion efficiency parameters are measured at 8 power levels (5%, 10%, 20%, 25%, 30%, 50%, 75% and 100%) normalized to the rated power.   + Determine the solar irradiance (W/m2) for the PV simulator using PRISMES software by feeding the calculated current, Idc for Umppmin, Umppnom and Umppmax values.   + A measurement dwell period of 10 minutes is considered for each of the power levels with 5 minutes of interval between the measurements.   + Prepare an irradiance profile for the each of the MPPT voltage and load it to PV simulator and wait untill the inverter synchronizes with the grid.   + Monitor the entire system for steady operations during the test period.   + Record the measured values of Udc, Idc, Uac and Iac at an interval of every second.   + The power conversion efficiency (Ƞconv) from the i*,* simultaneous measurements of Udc, Idc, Uac and Iac over a period ∆T as per the equation (1).     - = (1)   + The European power conversion efficiency (ȠconvEUR) and Californian power conversion efficiency (ȠconvCEC) can also be calculated using the equations (2) and (3).   ȠconvEUR = 0.03Ƞconv,5% + 0.06Ƞconv,10% + 0.13Ƞconv,20% + 0.1Ƞconv,30% + 0.48Ƞconv,50% + 0.2 Ƞconv,100% (2)    ȠconvCEC = 0.04Ƞconv,5% + 0.05Ƞconv,10% + 0.12Ƞconv,20% + 0.21Ƞconv,30% + 0.53Ƞconv,50% + 0.05 Ƞconv,100% (3)   * Over / Under Voltage and Frequency test (IEC /EN 61727 Grid code setting):   + To test the inverter for IEC/EN 61727 Metropolitan Electricity Authority (MEA) requirements: Manually adjust the Rotary switch A to position B and Rotary switch B to position 8 on the inverter underneath the LCD display board to set the right grid parameters compliant to IEC 61727. This can also be set remotely using dedicated portals by respective manufacturers.   + Design a logic diagram using Simulink tool on MATLAB to run the test in steps.   + Program the test steps for the below mentioned voltage and frequency levels allowing sufficient time in-between for the inverter to turn ON post dis-connection from the grid.   + Apply stable DC input from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.   + Allow some time for the inverter to synchronize with the grid parameters and turn ON.   + Monitor the entire system for steady operations during the test period.   + Record the real time voltage and current for all the 3 phases and frequency values at every 50µS time intervals and analyse the measured values.   + Determine the response/trip time and verify against the values stipulated in the standard. * Over / Under Voltage and Frequency test (Grid code parameter set to Default on DuT):   + An experimental test is carried out by keeping the grid code setting in Default setting (Rotary switch A and B at position 0) and compare the response time of an inverter against NRS 097-2-1:2017 requirements. This exercise is to understand the inverter response time during over or under voltage / frequency conditions when an installer leaves the grid parameter setting under default condition during commissioning (can happen mostly in developing countries like South Africa or any other).   + Design logic diagrams and program the test steps as explained in the earlier test for EN61727 grid code setting.   + Apply stable DC input from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.   + Allow some time for the inverter to synchronize with the grid parameters and turn ON.   + Monitor the entire system for steady operations during the test period.   + Record the real time voltage and current for all the 3 phases and frequency values at every 50µS time intervals and analyse the measured values.   + Determine the response/trip time and verify against the values stipulated in the standard. * Ride through functionality test:   + Design a logic diagram using Simulink tool on MATLAB to run the test in steps.   + Program the test steps for the below mentioned voltage ride through levels allowing sufficient time for the inverter to turn ON post dis-connections from the grid if any.   + Apply stable DC input from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.   + Allow some time for the inverter to synchronize with the grid parameters and turn ON.   + Monitor the entire system for steady operations during the test period.   + Record the real time voltage and current for all the 3 phases and frequency values at every 50µS time intervals and analyse the measured values.   + Determine the response/trip time and verify against the values stipulated in the standard. * Harmonic measurements:   + Perform measurement of Harmonic distortions in the current waveform for a full clear and cloudy sky day conditions. This test is also conducted without any load connected in the circuit.   + Design a logic diagram using Simulink tool on MATLAB to run the test continuously and load it to the grid simulator.   + Install a power quality analyzer and connect the voltage and current measurement probes of the Power Analyzer (PA) to the inverter output terminations.   + Prepare solar irradiance profile consisting 30 sec interval for a full day and program the PV simulator to feed the DC power continuously based on the irradiance.   + Keep the per phase AC power output limited to 4000W totalling to 12000W feeding to the grid.   + Calculate the Resistance (R), Inductance (L) and Capacitance (C) values for the RLC load bank using below equations and apply it to the load bank.   R = V2 RMS / P (4)  L = V2RMS / 2πfPQf (5)  C = PQf / 2πfV2RMS (6)  Where Qf = R = 1   * + Apply the programmed DC voltage and current inputs based on solar irradiance data from the PV simulator. Control the grid simulator and perform the required simulations using OPAL-RT real time simulation software.   + Monitor the entire system for steady operations during the test period.   + Record the voltage, current, frequency and harmonic emissions upto 50th order (3 kHz) at every second interval.   + Analyze and calculate the Total Harmonic Distortions (THDi) and Odd/Even harmonics for multiple orders for the current using the equation (7)   THDi = (7)   * + Verify the measured values against the requirements stipulated in EN 61727. * Islanding test:   + IEC/EN 62116 standard stipulates to subject the inverter to an islanding condition with active and reactive power test conditions (%) ranging as per the below table and at >90%, 50%±10% and <10% of the rated Vmpp.   + The test passes if both the following results for the recorded run-up time are satisfied:     - It has to be less than 2s in each transient;     - Each unbalanced condition of the grey shaded area of Table (6), it has to be less than that in the balanced one (cell 0, 0); if not, the tests must be extended to the un-grey shaded area.   + Due to limitation in time, only one test condition scenario where active power of generation to load is -5% and reactive power at +5% is simulated and tested.   + In this test, the per phase AC power output is limited to 3000W totalling to 9000W in the system.   + Calculate the Resistance (R), Inductance (L) and Capacitance (C) values for the RLC load bank using the equations (4) (5) and (6) and apply it to the load bank.   + Design a logic diagram using Simulink tool on MATLAB to run the test with a possibility to cut the power supply from the grid and load it to the grid simulator.   + Inject a stable DC power from the PV simulator to the inverter to keep the inverter synchronised and feeding power to the loads continuously.   + Trigger a grid failure situation using OPAL-RT real time simulation software and create an islanded condition with the active and reactive power levels at -5% and 5% respectively.   + Monitor the entire system for operation and record the AC voltage, AC current, active and reactive power on 50µS intervals and analyse the measured results.   + Determine the response time post grid failure and verify against the values stipulated in the standard. |

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| 1. **MAIN ACHIEVEMENTS** (results, conclusions, lessons learned) |
| * Power conversion efficiency test * The power conversion efficiency (Ƞconv) is carried out as per the methodology briefed in section 4.2. Figure 4 presents the calculated efficiency from the measured DC and AC power for Umppmin, Umppnom and Umppmax.     Figure 4: Power conversion efficiency measured at min, nom and max MPPT voltages   * Table (7) presents the measured Power conversion efficiency (Ƞconv), European power conversion efficiency (ȠconvEUR) and Californian power conversion efficiency (ȠconvCEC).  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | |  | **Ƞconv** | | | | | | | | **(Ƞcov EUR)** | **(Ƞconv**  **CEC)** | | 5% | 10% | 15% | 25% | 30% | 50% | 75% | 100% | | **Umpp**  **Min = 390V** | 0.94 | 0.96 | 0.97 | 0.97 | 0.97 | 0.97 | 0.96 | 0.96 | 0.96 | 0.97 | | **Umpp nom 600V** | 0.96 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | 0.97 | | **Umpp max = 800V** | 0.97 | 0.97 | 0.98 | 0.98 | 0.98 | 0.98 | 0.97 | 0.97 | 0.97 | 0.98 |   Table 2: Measured Ƞconv, ȠconvEUR and ȠconvCEC of theDuT   * Over / Under voltage test (IEC/EN 61727 Grid code parameters set on the DuT) * The response time of the DuT is measured as per the methodology briefed in section 4.2 of this report and compared against the values stipulated in IEC / EN 61727. Table (8) presents the measured results. The measured response time of all the voltage and frequency ranges is observed to be well within the stipulated time frames.  |  |  |  | | --- | --- | --- | | **Voltage Range**  **(At PoC)** | **IEC/EN 61727**  **Response time (secs)** | **Measured response time (secs)** | | V < 50% | 0.1 | 0.086 | | 50% ≤ V <85% | 2.0 | 1.998 | | 85% ≤ V ≤ 110% | Continuous operation | Continuous operation | | 110% < V < 135% | 2.0 | 1.963 | | V ≥ 135% | 0.05 | 0.053 | | **Frequency Range** |  |  | | >49Hz | 0.2 | 0.006 | | >51Hz | 0.2 | 0.011 |   Table 3: Measured Vs IEC/EN 61727 response time comparision   * The DuT re-connection time is measured post trip during an over / under voltage and frequency scenario. The time taken by DUT to connect back to the grid after the voltage and frequency returned to normalcy is presented in Table (9).  |  |  | | --- | --- | | **Trip trigger points** | **Re-connection time post trip** | | V < 50% | 132.60 | | 50% ≤ V <85% | 135.71 | | 110% < V < 135% | 132.04 | | V ≥ 135% | 135.89 | | **Frequency Range** |  | | >49Hz | 134.76 | | >51Hz | 132.68 |   Table 4: Re-connection time of the DuT post trip   * The real time plots in Figure (5) to (16) presents the measured time in more detail for each of the test case mentioned in Table (3) and (4).     Figure 5: Response time for the over voltage exceeding 110% of the VRMS    Figure 6: Re-connection time post trip during over voltage exceeding 110% of VRMS    Figure 7: Response time for the over voltage exceeding 135% of the VRMS    Figure 8: Re-connection time post trip during over voltage exceeding 110% of VRMS    Figure 9: Response time for the under voltage exceeding 85% of VRMS    Figure 10: Re-connection time post trip during under voltage exceeding 85% of VRMS    Figure 11: Response time for the under voltage exceeding 50% of the VRMS    Figure 12: Re-connection time post trip during under voltage exceeding 50% of VRMS    Figure 13: Response time for the under frequency exceeding 49Hz    Figure 14: Re-connection time post trip during under frequency exceeding 49Hz    Figure 15: Response time for the over frequency exceeding 51Hz    Figure 16: Re-connection time post trip during over frequency exceeding 51Hz   * Over / Under voltage test (Grid code parameters set to Default on the DuT) * The response time of the DuT is measured as per the methodology briefed in section 4.2 of this report and compared against the values stipulated in NRS097-2-1. Table (8) presents the measured results and it is observed at couple of voltage ranges, the measured results are outside the boundary limits. The measured results raise serious concerns when an installer does not set up the correct grid code applicable to the country and commissions the project with “Default” setting.  |  |  |  | | --- | --- | --- | | **Voltage Range**  **(At PoC)** | **Response time (secs)** | **Measured time (secs)** | | V < 50% | 0.2 | Trips before the voltage level can be taken to 50% | | 50% ≤ V <85% | 10 | 34.08 | | 85% ≤ V ≤ 110% | Continuous operation | Continuous operation | | 110% < V < 115% | 40 | 26.53 | | 115% ≤ V < 120% | 2 | 0.196 | | V ≥ 120% | 0.16 | 0.183 | | **Frequency Range** |  |  | | <47 Hz | 0.2 | 591.10 | | 47 ≤ Hz ≤ 50.5 Hz | Continuous operation | Continuous operation | | 50.5 ≥ Hz ≥ 52 Hz | Active power shall not increase and shall drop at a gradient of 50% per Hz | No increase in power, power drop starts only at 51Hz | | >52Hz | 0.5 | 0.04 |   Table 5: Measured Vs NRS 097-2-1 response time comparision   * The real time plots in Figure (17) to (27) presents the measured time in more detail for each of the test case mentioned in Table (5).     Figure 17: Response time for the under voltage exceeding 85% of the VRMS    Figure 18: Continuous operation of DuT during above 85% and below 110% of the VRMS    Figure 19: Response time for the over voltage exceeding 110% of the VRMS    Figure 20: Response time for the over voltage exceeding 115% of the VRMS    Figure 21: Response time for the over voltage exceeding 120% of the VRMS    Figure 22: Response time for the under frequency exceeding 47Hz    Figure 23: Continuous operation for the frequency 47Hz to 50.5Hz    Figure 24: Status of Voltage with increasing frequency from 50.5Hz to 52Hz    Figure 25: Status of Current with increasing frequency from 50.5Hz to 52Hz    Figure 26: Gradient of power during frequency increase from 50.5 to 52Hz    Figure 27: Response time for the under frequency exceeding 52Hz   * Ride through functionality test * The ride through functionality of the DuT during short term voltage dips is tested as per the methodology briefed in section 4.2. The monitored status for each of the voltage dip is presented in the table (6).  |  |  |  |  | | --- | --- | --- | --- | | **Dip type** | **Ride through voltage levels** | **Duration** | **Monitored status** | | Y type | 10% ≤ V ≤ 15% | 2000 ms | Ride through | | Y type | 15% ≤ V ≤ 20% | 600 ms | Ride through | | Y type | 20% ≤ V ≤ 30% | 150 ms | Ride through | | X1 type | 30% ≤ V ≤ 40% | 150 ms | Ride through |   Table 6: Monitored Vs IEC/EN 61727 requirement   * The real time plots in Figure (28) to (31) presents the ride through functioning by DuT for the duration specified during different voltage levels as mentioned in Table (6).     Figure 28: DuT ride through functionality during 15% voltage dip for 2000mS    Figure 29: DuT ride through functionality during 20% voltage dip for 600mS    Figure 30: DuT ride through functionality during 30% voltage dip for 150mS    Figure 31: DuT ride through functionality during 40% voltage dip for 150mS   * Harmonic measurements: * The total harmonic distortions measurement is carried out as per the steps briefed in section 4.2. The measured fundamental AC current (I ph) for all the 3 phases is plotted against the solar irradiance profile and is presented in Figure (32). * A good overlay of the generation profile of current over irradiance indicate there are no outliers in the measurement and the harmonics outcome can be co-related to irradiance conditions or turn ON of OFF periods. * Figures (33) to (39) presents the measured THD, Odd harmonic distortions for orders 3rd to 9th, 11th to 15th, 17 to 21st and 23rd to 33rd, Even harmonics distortions for orders 2nd to 8th and 10th to 32rd for all the 3 phases for a clear and cloudy sky irradiance profiles. * A high THD in all 3 phases is observed for both the sky conditions during early and late sun hours of the day i.e. period when an inverter tends to turn ON with increasing irradiance and tending to turn OFF when the irradiance levels are dipping sharply at the end of the day. * The measured THD is well above the requirement of 5% in the EN61727 standard. * The THD measured for a cloudy day profile is also higher than the clear day and crosses the maximum limit of 5%. * Similar results are observed for the rest of the odd orders from 3rd to 9th, 11th to 15th, 17th to 21st and 23rd to 33rd and even orders of 2nd to 8th and 10th to 32rd. * It is also observed that some of the harmonics in the network is absorbed by the filters in the inverter during the course of the day or peak power generations.     Figure 32: Overlay of measured fundamental current for 3 phases over clear and cloudy irradiance profiles    Figure 33: THD measured for clear and cloudy day irradiance profile    Figure 34: Harmonic distortions measured for the odd orders from 3rd to 9th    Figure 35: Harmonic distortions measured for the odd orders from 11th to 15th    Figure 36: Harmonic distortions measured for the odd orders from 17th to 21st    Figure 37: Harmonic distortions measured for the odd orders from 23rd to 33rd    Figure 38: Harmonic distortions measured for the even orders from 2nd to 8th    Figure 39: Harmonic distortions measured for the odd orders from 10th to 32nd   * Islanding test: * An attempt is made to verify the anti-islanding functionality of the solar inverter when the active power of generation to load ratio is -5% and the reactive power is at +5%. * It is noted during the exercise that the test is repeated for many combinations of active and reactive power as briefed in section 4.2. * It is also understood that to reach the active and reactive power to the specified ratios as per the standard consumes more time and a precise and sophisticated test infrastructure to carry out the islanding test. * Figure (40) presents the status of voltage, current, active and reactive power during the test. The active power in the network is balanced to -5.6% and due to time limitations, reactive power could not be balanced to 5% as per the standard requirement. * Figure (41) presents the measured trip time after the loss of grid when the active power of generation to load is at -5%. * The time taken by the inverter to check the loss of the grid and stop supplying the power to the closely matched demand by the loads is 0.108secs which is well within the limit of 2s specified in IEC/EN standard 62116. * It is noted that it is a learning activity and further efforts will be made in the future to balance the active and reactive power as per Table (6) and repeat the tests to determine more meaningful test results.     Figure 40: Measured voltage, current, active and reactive power during islanding test    Figure 41: Response time of DuT during islanded condition |

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| 1. **PLANNED DISSEMINATION OF RESULTS** (journals, conferences, others) |
| The exposure to real time inverter characterization at CEA-INES laboratory has certainly enhanced our know how on the configurations and protection system within the inverter, test infrastructure, test procedures, deep dive into the protocols per standards, real time measurements and validation of test results. The experience will position us to establish our own inverter characterization facility above our existing solar PV module and battery storage characterization facilities within the institution.  The results obtained during this program will be published at one of the conferences or workshops scheduled within the country during the calendar year 2020. The experience gained during this program will be disseminated to colleagues, students and other interested parties during our scheduled monthly meetings or brown-bag sessions. |

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| 1. **PLANNED DISSEMINATION OF RESULTS** **THROUGH ERIGRID CHANNELS**   Contact [erigrid-ta@list.ait.ac.at](mailto:erigrid-ta@list.ait.ac.at) to organise promotion of your results |
| I am open to present the work if it is beneficial to any audience anywhere and look forward to further communications on ERIGrid channels and sponsoring information’s from the ERIGrid.  I am very thankful to ERIGrid for granting this wonderful opportunity to access the program, use test infrastructure at one of the base and get to know insights of inverter characterization. I also thank Prof. Tuan Quoc Tran, Mr. Van Hoa Nguyen and Mr. Marc Jung for all the support provided during my stay at CEA-INES. |