TRANSNATIONAL ACCESS
USER PROJECT FACT SHEET

USER PROJECT	
Acronym	**PERSEID**
Title	**Modeling and stability analysis tools to contribute to the high Penetration of powER electronicS convErters In the Distribution power systems**
ERIGrid Reference	**04.022-2018**
TA Call No.	**4th**

HOST RESEARCH INFRASTRUCTURE			
Name	**SINTEF: National Smart Grid Laboratory (NSGL)**		
Country	**Norway**		
Start date	**24/04/2019**	**Nº of Access days**	**18**
End date	**24/05/2019**	**Nº of Stay days**	**31**

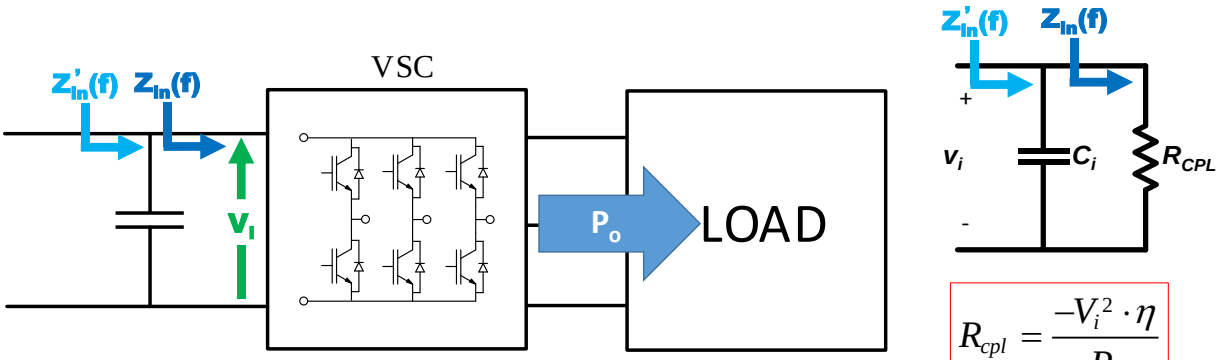
USER GROUP	
Name (Leader)	**Clara Marina Sanz García**
Organization (Leader)	**Universidad Carlos III de Madrid**
Country (Leader)	**Spain**
Name	**Francisco Huerta Sánchez**
Organization	**Universidad Carlos III de Madrid**
Country	**Spain**
Name	**Daniel Santamargarita Mayor**
Organization	**Universidad Carlos III de Madrid**
Country	**Spain**

1. USER PROJECT SUMMARY (objectives, set-up, methodology, approach, motivation)

The main goal of this project is to validate the proposed simple reduced-order input impedance models of power converters as well as generate a new generalized stability analysis based on the use of the reduced-order model.

This model can be used in the stability analysis of the DC bus when multiple source and load converters are connected, it can be used in complex distribution systems such as HVDC transmission systems or offshore power generation systems.

The model is based on the fact that a regulated power converter behaves as a constant power load. This behavior can be interpreted as a negative resistor.



$$R_{cpl} = \frac{-V_i^2 \cdot \eta}{P_o}$$

Therefore, the total impedance of the converter $Z_{in}'(s)$ can be obtained from the parallel of the negative resistor and the input capacitor of the converter.

$$Z_{in}'(s) = \frac{R_{CPL}}{1 + R_{CPL} \cdot C_i \cdot s}$$

In order to obtain the input impedance of the Voltage Source Converter (VSC) variable frequency disturbances must be introduced in the DC input voltage. To obtain the impedance, the input current disturbance must be measured and compared with the input voltage disturbance.

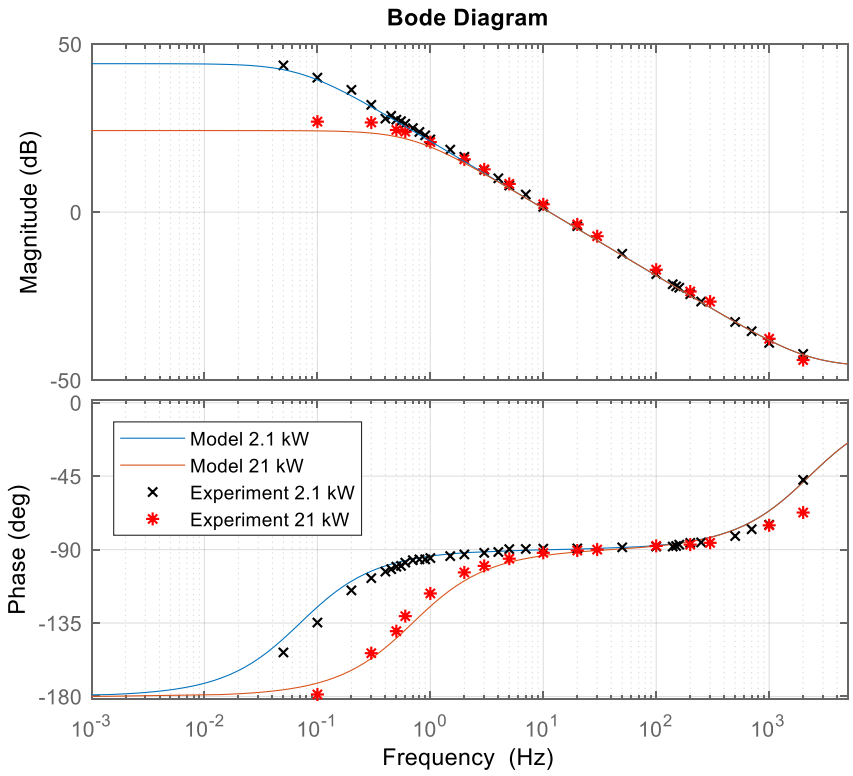
To validate the reduced order model two different types of tests will be done

- **Same power converter topology with different control strategies**: Used to determine if the control loop affects the converter impedance.
- **Different power converter topology**: Used to determine if the topology affects the converter input impedance.

2. MAIN ACHIEVEMENTS (results, conclusions, lessons learned)

The main achievement of the project has been the experimental validation of the reduced input impedance model for different powers, input voltages, input capacitors, and different controls.

The model validation has been performed using as a Two-Level Voltage Source Inverter (2L-VSC) topology with different loads, a resistive load and an active load. The following figure illustrates the type of results obtained in the tests that have been carried out at National Smart Grid Laboratory (NSGL). As seen the model have a very good accuracy in comparison with the experimental results.



As main conclusion, the results of the project allow to extend the applicability of the proposed reduced order model in many different high-power system applications. The test allows power system designers to perform system stability analyses in a faster and more efficient way since the proposed model only requires the value of the input capacitor of the converter as internal parameter. The rest of the parameters are estimated using the input voltage and the power delivered by the converter.

In addition, some lessons regarding practical issues of the setup have been also learned by the user group members and the SINTEF researchers during the test performed in collaboration at NSGL (see the figure below). Due to these practical issues some of the tests that deals with the test of other high-power inverter topologies, such as Modular Multilevel Converter (MMC) topology and controls, such as α β reference frame, cannot be properly performed during the stay at NSGL.

As summary, the results of this project contribute to avoid the need for complex modeling techniques or expensive measurements with frequency response analyzers to determine the impedance of the converter for performing systems stability analysis in real applications.

3. PLANNED DISSEMINATION OF RESULTS (journals, conferences, others)

It is planned to prepare different scientific publications in several conferences and journals. As prestigious conferences in the field, we have already submitted some results of the project in conference papers.

One paper has been accepted at SAAEI 2019 and another paper is under review at IECON 2019. In addition, it is also planned to send one paper to be published in prestigious journals in the field like IEEE Trans. on Power Electronics (IF: 7.151), IEEE Trans. on Industrial Electronics (IF: 7.168), IEEE Journal of Emerging and Selected Topics on Power Electronics (IF: 4.269) or Applied Energy (IF: 7.182).

Moreover, a detailed dissemination of all results will be included in the PhD thesis of Daniel Santamargarita. This thesis is also part of the CONEXPOT project (DPI2017-84572-C2-2-R) (AEI/FEDER, UE), which is a national project comprised of different academic partners with the aim of standardizing the design of the interconnected architectures, in order to develop new methods and tools that can aid in the analysis and design of these systems.

Finally, a reference of the project on the websites of the User Group Institution will be included.