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PERSEID

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[Rev. No 1]	Technical report summarizing the main tests, results and conclusions	M. Sanz F. Huerta D. Santamargarita	25.06.19
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Table of contents

Abbreviations

GMPM	Gain Margin Phase Margin
FRA	Frequency Response Analyser
CPL	Constant Power Load
DC-AC	Direct Current to Alternating Current
2L-VSC	Two Level Voltage Source Converter
MMC	Modular Multilevel Converter
PLL	Phase Locked Loop
FRA	Frequency Response Analyser
PWM	Pulse-Width Modulation
TA	Trans-national Access

Executive Summary

In recent years the need for DC distribution buses has increased considerably. These distribution buses are very useful in some systems such as the DC distribution buses of an aircraft or ship, the connections of HVDC offshore wind plants or the distribution buses of a microgrid. Given the complexities of the systems presented above, the need to use more and more switched power converters has arisen. The main problem of the connection of multiple controlled switched converters acting as source and load is the degradation of stability that occurs on the distribution bus due to the converter interactions. Therefore, the fact that the converters are standalone stable does not ensure the stability of the bus.

To study the stability in the distribution bus there are some well-established criteria, such as the *Middelbrook* criterion or the *GMPM* criterion. These criteria require knowledge of the input impedance of the converters that act as load and the output impedance of the equipment that acts as source. The impedance of the different converters can be obtained analytically as well as by means of experimental tests with an *FRA*, the analytical method is a time-consuming study and it is necessary to know the internal components of the converter, on the other hand, the method of the experimental obtaining with FRA does not take so much time, but it needs the use of very expensive systems, especially for high power converters.

In order to reduce the complexity of obtaining impedance, a reduced order model for closed loop input impedance has been proposed. this model is based on the fact that a controlled power converter behaves as a constant power load (*CPL*), this behaviour can be interpreted as a negative resistor. This model has multiple advantages such as that it can be obtained from very simple and short time-consuming measurements of the load converter: Input capacitor; input voltage; output power and efficiency. A prior knowledge of this input impedance can be very useful to properly design the control of the source converters and in this way achieve stability on the distribution bus.

The main objective of this stay is the validation of the model for high power *DC-AC* converters, for this purpose, input impedance measurements have been made for a *2L-VSC* with different controllers and different loads connected at the AC side, a *MMC* has also been tested to see if the change in converter topology affects the model. In order to obtain these measurements, a direct measurement similar to the one obtained with an *FRA* was made, EGSTON *grid emulator* was used to introduce a disturbance at different frequencies in the input voltage of the converter acting as load, with the measurements of the disturbed input voltage and current the experimental input impedance was obtained in a certain range of frequencies.

USER PROJECT	
User Project Acronym	**PERSEID**
User Project Title	**Modeling and stability analysis tools to contribute to the high Penetration of powER electronicS convErters In the Distribution power systems**
Main scientific/technical field	**Stability analysis, Power distribution, DC distribution, Impedances.**
Keywords (5 max., free text)	**Stability, Impedance study, Network, Distribution**
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Research Motivation

Due to the increasing use of power converters in DC distribution buses, it is becoming more necessary to obtain easier stability criteria. The proposed reduced order model has been developed to reduce the complexity and time of these studies, being able to quickly and accurately analyse the stability of the system, as long as the output impedance of the source converters is known. The motivation of this research is to detect the accuracy of the model and at the same time determine the limit where the model can be applied.

1 Objectives

The main objective is to obtain the precision of the model, this main objective is divided into the following partial objectives:

- ***1º Same power converter topology with different control strategies****: Used to determine if the control loop affects the converter impedance.*

- ***2º Different power converter topology****: Used to determine if the topology affects the converter impedance.*

For the first test it is important to check what happens when the control bandwidth changes, checking that a slow control does not distort the CPL zone of the impedance (low frequencies). the addition of an external control loop (PQ Control) to the internal current control loop has also been studied. Another important element to check is the effect that the PLL has on the impedance of the system, to check this, the grid connection has been replaced by a connection to a resistor bank, thus eliminating the need to use a PLL and using a fixed reference generator created inside the Opal RT.

2 Scope

The report explains the scenarios that are tested in the lab including some of the most interesting results explaining the testing methodology used to obtain them. Once the results have been obtained, they are compared with the reduced order model in order to validate the proper behaviour. All experiments were performed on the same converter, a DC-AC with 60 kVA 2L-VSC topology, controlled by a real-time simulator, Opal-RT OP5600-ML605.

High power tests have been performed using common control strategies, current control and power control, and using the reference axes commonly used for connecting an inverter to the grid, DQ reference axes.

3 State-of-the-Art

The increase in the number of controlled switched converters connected in parallel to the same DC distribution bus generates a degradation in the stability of that bus [1], making the bus unstable even though all the converters are independently designed to be standalone stable.

There are several methods to detect the stability in the interconnection, which are based on the study of impedances [2]. The connection of two individually stable systems can be modeled as the serial connection of the small signal output impedance of the source system Z_S and the small signal input impedance of the load system Z_L, Fig. 1. Resulting in the expression (1) of open loop in which the stability of the global system can be studied.

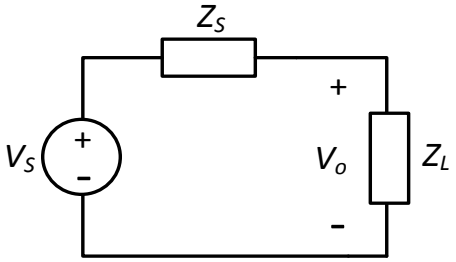

Fig. 1. Connection model of two systems based on their input and output impedances

$$T_{OpenLoop}(s) = \frac{Z_s(s)}{Z_L(s)} \quad (1)$$

So, it is necessary to know accurately the small signal impedances of all converters connected to the distribution bus, output impedance for converters that act as a source and input impedance for those that act as a load.

This stay has focused on the study of the input impedance. There are several methods to obtain the real input impedance:

- By means of an **analytical study** modelling the converter, its control, parasitic elements, etc. As it can be seen in [3] this process can be time consuming and it is necessary to know all the internal components of the converter, which is very difficult to do in commercial converters.

- It is possible to obtain experimentally the value of the closed-loop input impedance by means of a **FRA** [4]. This method requires highly expensive instrumentation, it is also problematic to measure high voltage and power equipment, as these converters usually have a very large input capacitor, so in order to observe the high frequency response it is necessary to introduce a disturbance of a very large amplitude into the input voltage.

- Using the **reduced order model** as it is explained below

Based on the fact that controlled converters that act as load have a constant power load (CPL) behaviour consuming a constant amount of power regardless what the input voltage is. This behaviour as a constant power load can be modelled in small signal as a negative resistance (2). Resulting in the equivalent total impedance (3) of the system shown in Fig. 2.

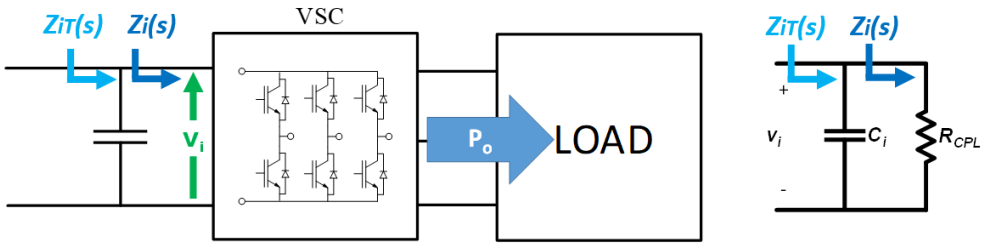

Fig. 2. Reduced model with CPL behaviour

$$R_{CPL} = \frac{-V_i^2 \cdot \eta}{P_o} \tag{2}$$

$$Z_{iT}(s) = \frac{R_{CPL}}{1 + R_{CPL} \cdot C_i \cdot s} \tag{3}$$

As you can see this model has many benefits over other ways of obtaining impedance. because it is only necessary to know the value of the input capacitor, the output power and the input voltage.

Precision studies of the model for DC-DC converters have already been carried out as can be seen in [5] and [6]. It was observed how the model correctly adapts to the actual input impedance as long as the bandwidth of the control is higher than the pole that introduces the input capacitor of the load system into the input impedance.

The input impedance of DC-AC converters has been studied along the stay. During this report the validation of the use of the model for DC-AC converters will be shown.

4 Executed Tests and Experiments

Five main tests have been carried out for the project:

- Different powers
- Different input capacitors
- Different controls
- Change of load type (grid or resistive)
- Negative reference use

In order to perform these tests, the converter was fixed at a working point and then the disturbances were introduced. All these tests have been carried out with the same inverter.

4.1 Test Plan

To obtain the input impedance of the closed-loop converter, a method equivalent to that used by FRAs has been applied. It will therefore be necessary to introduce a disturbance in the input voltage of the converter and measure this voltage and the input current resulting from the disturbance.

In order to do this, the following steps are required:

Step 1: <u>Make the hardware connections</u>

make the physical connections of the converter to the grid emulator on the AC side as well as on the DC side. When a grid connection is needed, the grid emulator will supply the DC voltage and set the AC voltage. However, when a connection to a resistive load (resistor bank) is required, the grid emulator will only supply the DC voltage. An example of the laboratory connection made for an active load (grid) is shown in the Fig. 3.

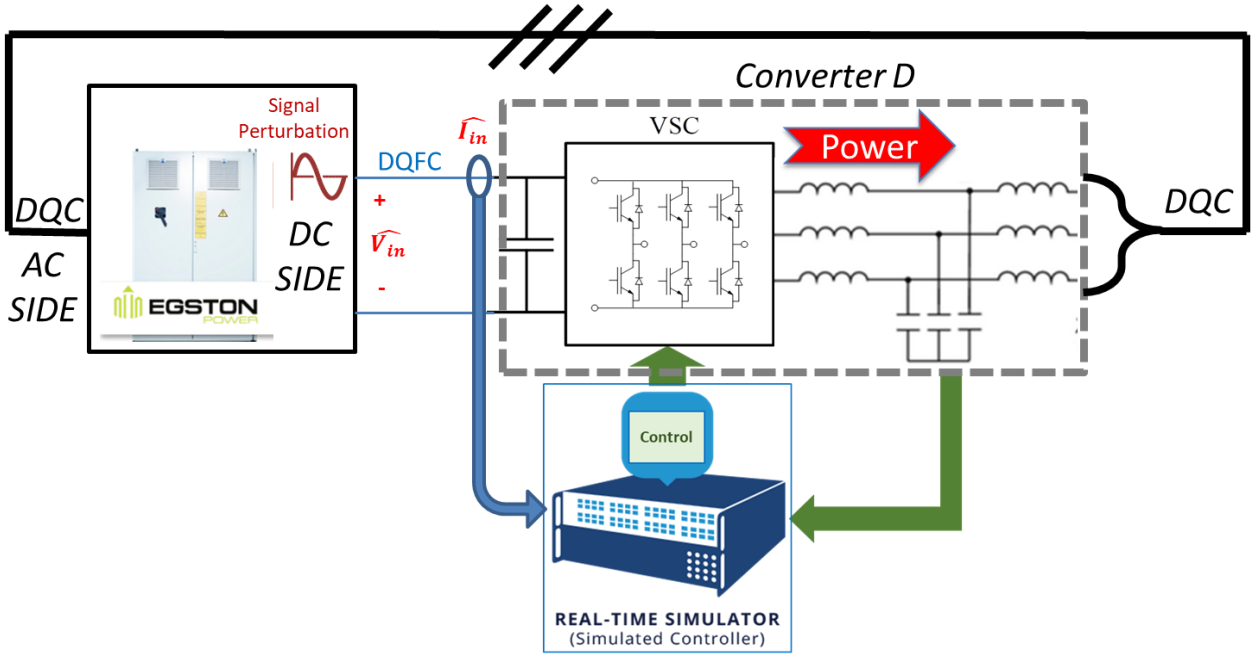

Fig. 3. Connection in the laboratory for the case study of a grid connection

Step 2: Configure the external systems

Once the physical connections have been made it is necessary to communicate with the network emulator to indicate which connections are going to be used both on the dc side and on the ac side. To control the dedicated computers for the EGSTON grid emulator and the OPAL-RT on one screen, team viewer program was used.

Step 3: Set the operating point of the converter and for the external systems

The converter is controlled by the real-time simulator Opal-RT, this simulator has both FPGA and processor, which allows to introduce controls and simulations with a short time step. It is possible to program this system using Simulink, so graphic control interfaces can be used.

Therefore, for this step the compiled control program will be loaded to the Opal-RT. First of all, set the voltages to be supplied by the grid emulator, once the voltages have stabilized the controller will be enabled and the breakers will be closed. Once the PLL has been synchronized (network connection case) the operating point will be set and wait until the system has stabilized.

Step 4: Introduce the disturbance and save the data

To introduce the disturbance, the Simulink file that set the voltage reference on the DC bus was modified, adding a sine wave of variable amplitude and frequency to the constant DC voltage reference. Due to the shape of the impedance, a look up table was created to modify the amplitude of the input voltage disturbance for each frequency, because if the amplitude of the disturbance were kept constant at all frequencies, the amplitude disturbance of the input current would increase too much at high frequencies. Fig. 4.

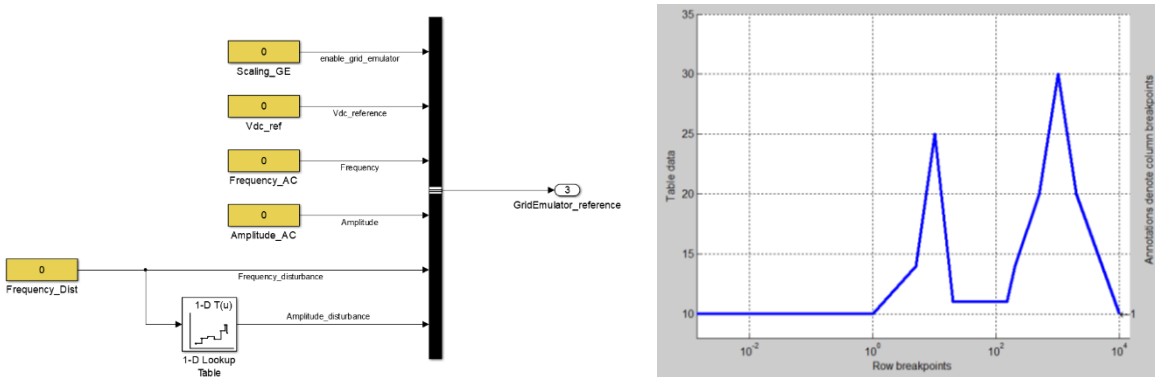

Fig. 4. Way of introducing the disturbance and example of a look up table used

A current probe and a voltage difference probe were used as redundancies to the measurements from OPAL-RT and the data were obtained by means of an oscilloscope.

Step 5: Data processing

Once the data is stored in frequency-separated files, it is processed independently using FFT algorithms to obtain the magnitude of the impedance. To obtain the phase, algorithms that are able to obtain the phase difference between the voltage signal and the current signal were applied.

The methodology explained above has been used for all the cases described below.

4.2 Test Set-up(s)

4.2.1 Implementation details

In Fig. 3 the connection scheme of the converter to the rest of the elements of the system is shown. The Table. 1 below shows the value of the inverter input filter and output filter.

Parameter	Value
Cin	14.1 mF
Rcin	0.005 Ω
Lfiltconv	0.5 mH
Cfilt	50 µF
LfiltGrid	0.2 mH

Table. 1. Real inverter filter parameters

Fig. 5 shows an example of how the control program loaded in the Opal-RT is structured

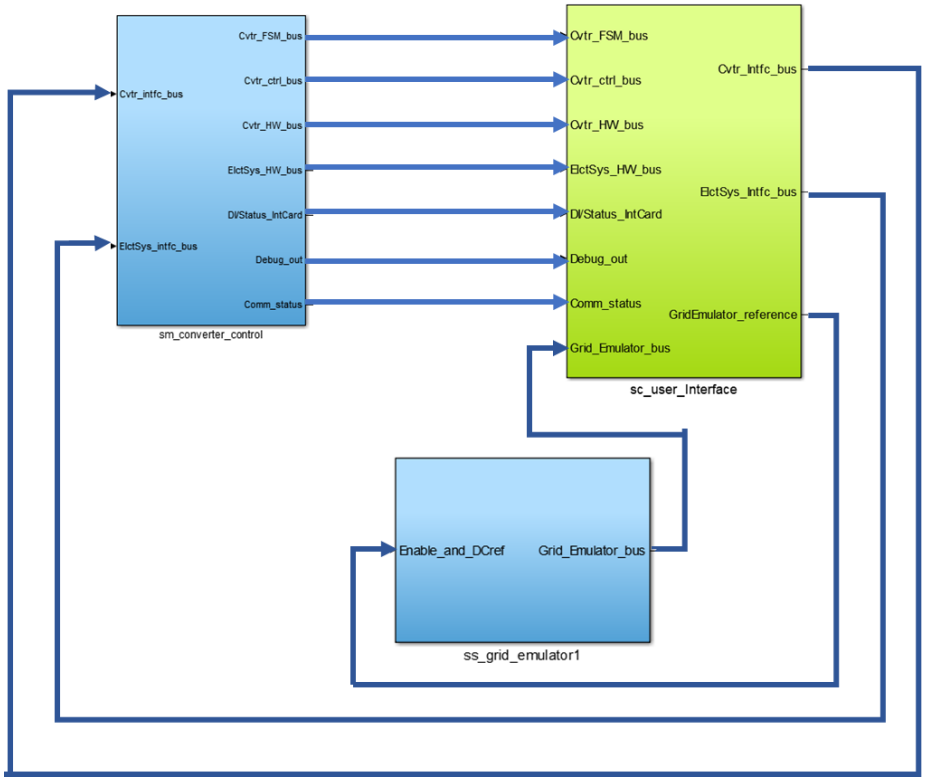

Fig. 5. Simulink file used for real-time simulation

Fig. 5 shows the Simulink program used to perform the simulation in real time. Three main subsystems can be clearly differentiated in this file:

- **Sm_converter_control**
- **Ss_grid_emulator**
- **Sc_user_interface**

The first two are compiled and run inside the OPAL-RT while the last one runs inside the interfacing computer. The purpose of each of the subsystems mentioned before is explained in detail below.

Sm_converter_control

Within this subsystem the connection with the converter, the measurements of the sensors, the protections, the control and the generation of the switching signals (PWM) are carried out. The control that has been carried out is a PI control, for which the reference axes DQ are used. Decoupling is applied to the D and Q currents, a feedforward of the supply voltage and an active damping are also applied. This active damping is necessary when having an LCL filter. Fig. 6 shows how the current control, the axis decoupling and the feedforward of the input voltage have been carried out.

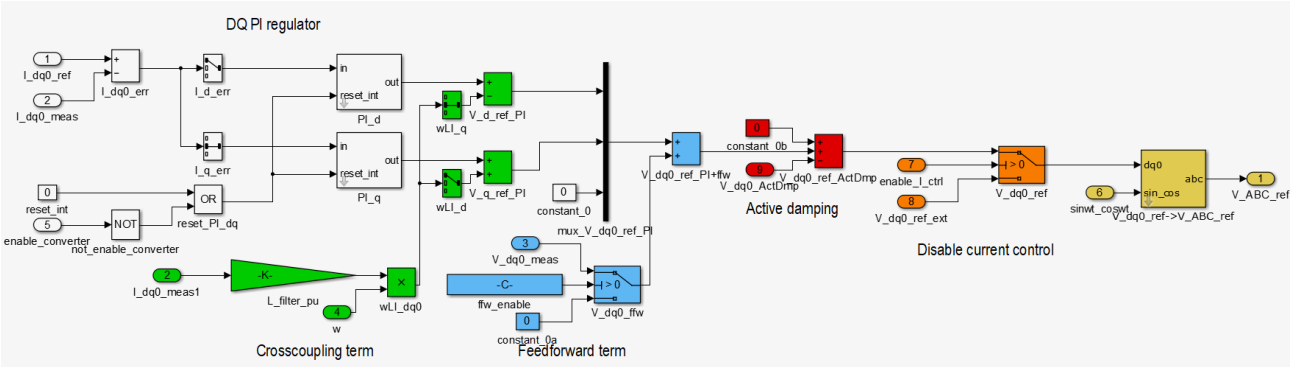

Fig. 6. Current control used in the real-time simulator.

Ss_grid_emulator

In this subsystem the connection with the Egston grid emulator is made, sending the DC and AC voltage references. As in this case the DC voltage reference is not constant, it is necessary to introduce a disturbance on the constant voltage. In the Fig. 7 it can be seen how the disturbance has been implemented.

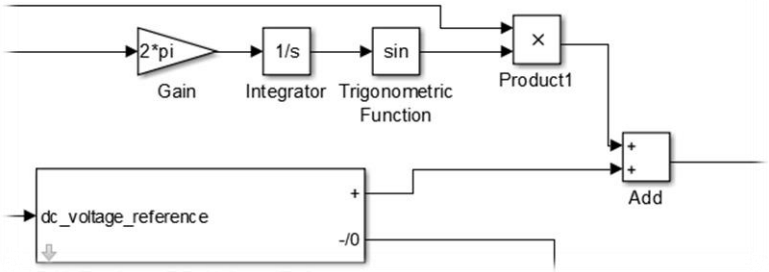

Fig. 7. Way to generate the input voltage disturbance

This generator receives the frequency and amplitude references from the *Sc_user_interface* subsystem so it is possible to change them manually. Because if they were introduced in the current subsystem when it is in the FPGA it would not be possible to modify these values manually.

Sc_user_interface

This subsystem goes inside the processor and is in charge of communicating with the computer and displaying the graphical interface and the scopes.

4.2.2 Equipment and Communications Involved

The Egston grid emulator (Fig. 8) is used to generate the voltage buses. This emulator can provide a power of 100 kVA.

Fig. 8. Egston Grid Emulator

The 2L-VSC inverter (Fig. 9) has been designed in the NSGL laboratory, so it is not a commercial converter. This converter communicates with the Opal-RT via fiber optics. The switching frequency used was 5 kHz.

Fig. 9. 2L-VSC inverter

All measurements have been taken with a differential voltage probe, an amperimetric probe and the tektronix oscilloscope shown in the Fig. 10.

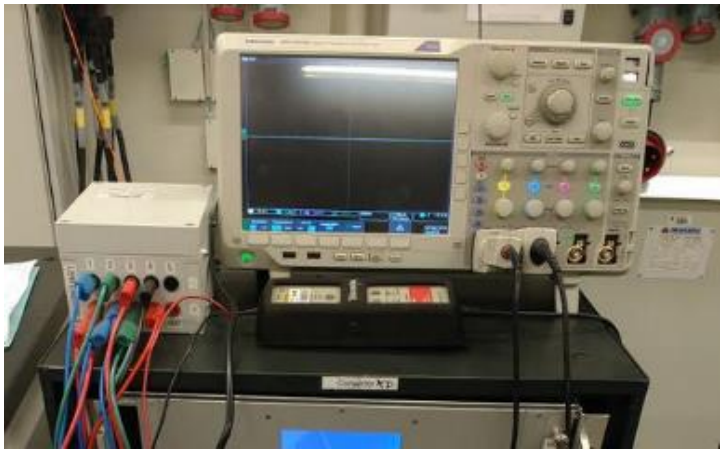

Fig. 10. Tektronix oscilloscope used to take measurements

To carry out the communication and control of all the equipment, Opal-RT version OP5600-ML605 was used, it was connected by optical fiber, Fig. 11.

Fig. 11. Opal-RT OP5600-ML605

4.2.3 monitoring aspects

It was determined that in order to have more control over the measurement results, samples would be taken point by point, in the beginning it was obtained by a more automatic process taking the data from the sensors of the converter from the Opal-RT, the problem is that they did not have enough resolution for the voltage and current ranges that were being measured. Finally, a current probe and a voltage difference probe were used and the data were obtained by means of an oscilloscope.

In the Fig. 12 it can be seen a comparison between the voltage disturbance measured by the sensors of the converter and another measure through the grid emulator, it is possible to see how the sensors of the converter have a lower resolution than those present in the grid emulator giving as a result an square voltage. The difference in the phase and amplitude of both signal is also due to the effect of the cable used in the connection as it is detailed below.

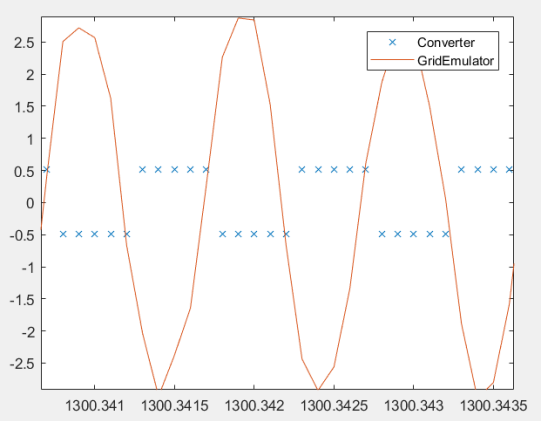

Fig. 12. Comparison between the measured voltage in the grid emulator and the measured voltage in the converter

It would be better to measure the output voltage directly with the grid emulator and save these values with the Opal-RT. The problem with this is that the connection between the grid emulator and the converter is made with a cable of approximately 10 meters long, this cable introduces into the total system an inductance that would affect the final impedance, as can be seen in the Fig. 13.

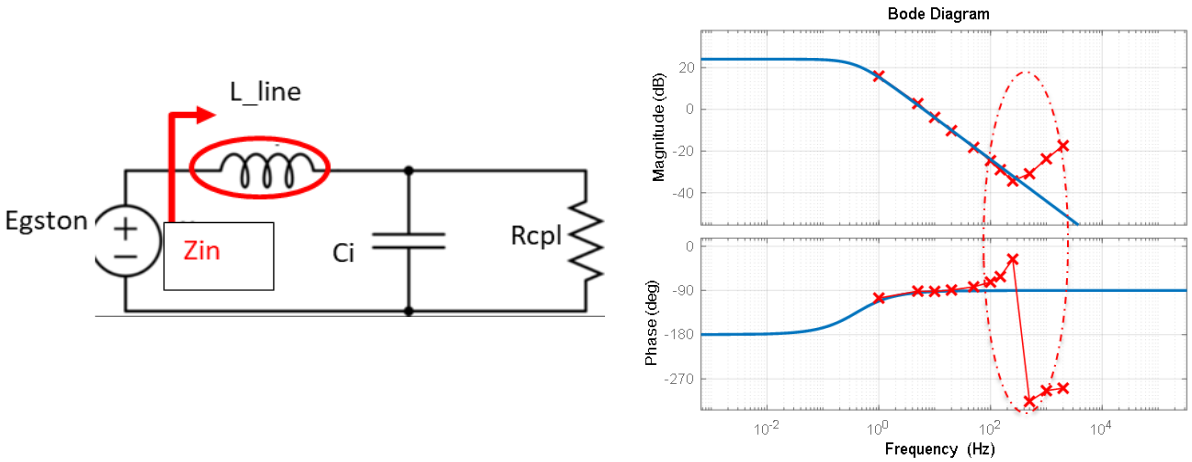

Fig. 13. Schematic of the inductance introduced by the line and effect on the real impedance

As it can be seen in the previous figure the processing of the data using the measurements of the Egston grid emulator is not correct since the effect of the inductance of the line is introduced. To be sure of this affirmation the theoretical equation of the inductance of a line was used and the obtained was compared with the extrapolated inductance of the input impedance obtained. As can be seen in the results obtained (4) and (5) the statements are correct.

$$L = 0.2 \cdot leng \cdot \left(\ln\left(\frac{4 \cdot leng}{d}\right) - 75\right) = 15.08\ \mu H \tag{4}$$

$$Z_{in} = j\omega L_{line} + \frac{1}{j\omega C_{in}} = \frac{(j\omega)^2 L_{line} C_{in} + 1}{j\omega C_{in}} \rightarrow L_{line} = 11.7\ \mu H \tag{5}$$

**The impedance of (5) has been calculated assuming that there is no load on the converter*

4.3 Data Management and Processing

As mentioned before, the data were finally taken with the oscilloscope, in order to obtain the file with the data shown on the screen, the "*Tektronix Openchoice Desktop Application TDSPCS1"* was used. In our case a CSV file was saved for each frequency to be analysed, later these files were processed with Matlab. The same number of data, 10000 points, was taken for all cases, so that the processing of the data would be simpler in the future. At all frequencies, an attempt was made to take as many cycles as possible in order to obtain the best results when performing FFT analysis, taking into account time restrictions, since when perturbations were made at a very low frequency of 0.01 Hz, taking 10 cycles meant excessively long time. An example of data acquisition can be seen in the Fig. 14.

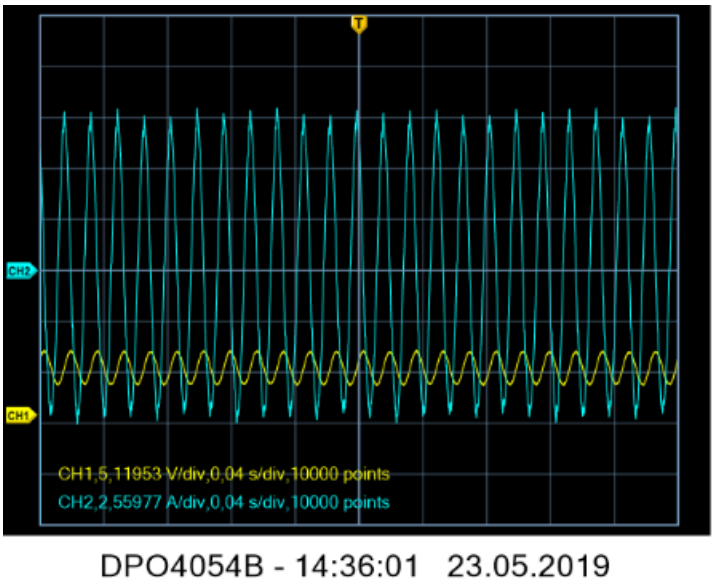

Fig. 14. Example of the voltage (yellow) and current (blue) data taken with the oscilloscope (Test 20 kW current control)

In order to have the data organized, an array was generated for each frequency. once all the data are ordered, the data are processed, in order to obtain the magnitude of the impedance, the bilateral spectrum at a certain frequency is obtained from the current and the voltage separately. In the Fig. 15 it can be seen how is the bilateral voltage spectrum for a disturbance of 1 Hz.

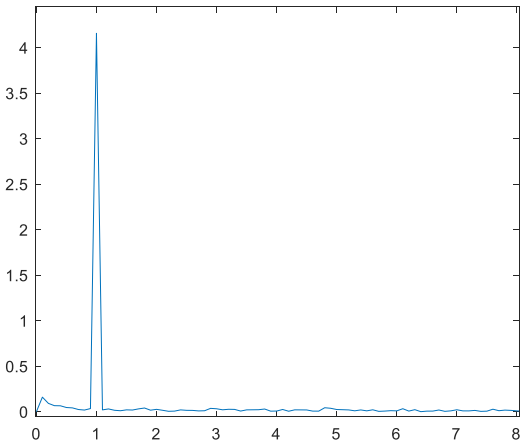

Fig. 15. Bilateral spectrum of disturbance at input voltage for 1 Hz

As can be seen in figure 15 the spectrum does not show continuous component, this has been removed previously by the Matlab "*detrend"* function. Once the bilateral spectrum has been obtained, the maximum value and its frequency is saved. Same processing is performed for current and voltage, once the maximum magnitude is obtained at a certain frequency the voltage is divided by the current to obtain the input impedance (6).

$$\widehat{Zi} = \frac{\widehat{Vi}}{\widehat{Ii}} \tag{6}$$

The result of this division is expressed in natural gain, so it is necessary to convert it to dB by applying the logarithm in base 10 of the value and then multiplying it by 20.

In order to obtain the impedance phase, it is necessary to measure the phase difference between the voltage and the current, for this purpose the "*phdiffmeasure"* function is used.

5 Results and Conclusions

Throughout this section the main different tests carried out during the stay will be discussed, after each test a small comment will be made as a particular conclusion, finally final conclusions will be made about the suitability of the reduced order model of the input impedance of the inverter. In all tests, the results obtained experimentally will be compared with the reduced order model. **Unless otherwise indicated, the connection used will be as shown in the Fig. 3. Having a grid voltage of 400 V.**

5.1 Comparison between different input capacitors *Ci (Grid connection, Current control, DQ)*

At the beginning of the experiments there was another converter connected to the DC power bus, although this converter was turned off and did not demand power, the input capacitor of this was in parallel with the converter we were studying, so the value of the effective capacitor varied as can be seen in the Fig. 16.

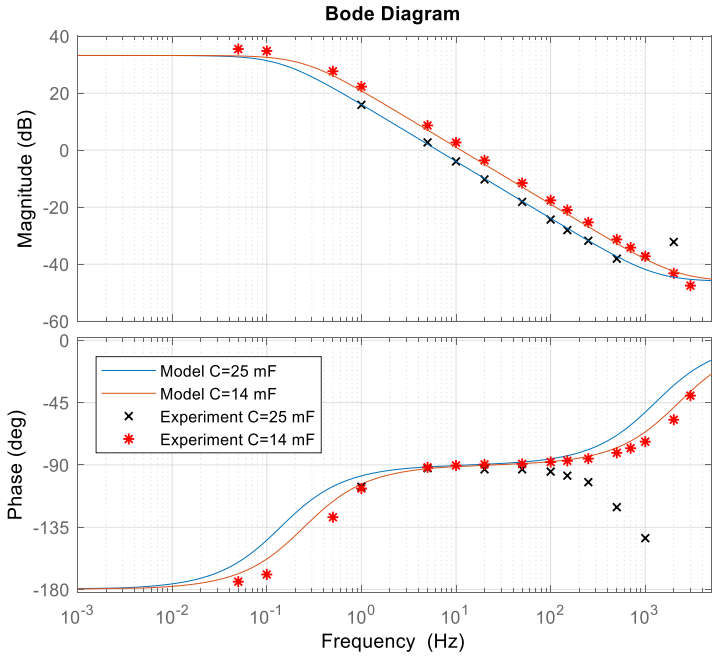

Fig. 16. Closed-loop input impedance comparison for two input capacitor values.

(Vi=150 V, Po=400 W)

It is necessary to emphasize that the experiment with the effective 25 mF capacitor was the first experiment that was performed, so it was not measured with the oscilloscope but it was measured with the Opal-RT. As mentioned above the measurements made with the Opal RT have problems with resolution, so the errors in the high frequency phase are due to that. On the other hand, the magnitude does not present so many errors as the phase since we only keep the main harmonic and the rest are ignored.

This first test was carried out at a very low input voltage and power, but it is useful to check how **the model correctly detects the changes produced in the input capacitor**.

5.2 Comparison between different output power *Po (Grid connection, Current control, DQ)*

For the next test, the rest of the converters connected to the bus have been disconnected and the input voltage has been raised to 700V to work with real operating cases. This test shows the input impedance for 2 different powers 2.1 kW and 21 kW. I**n this case the control carried out was similar to the current control shown in the Fig. 6.**

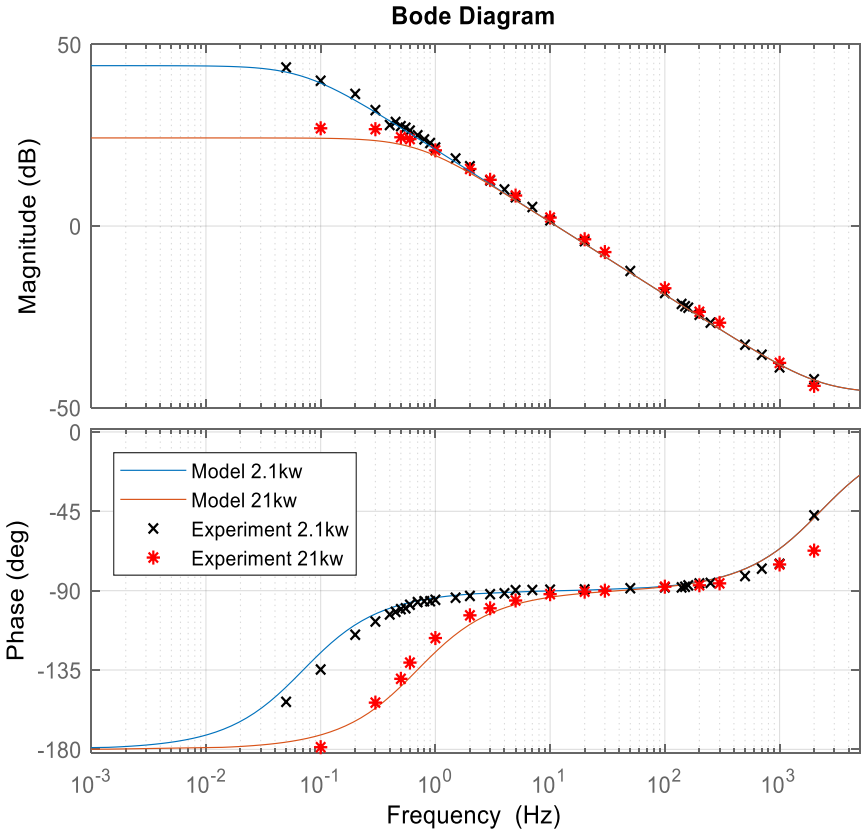

Fig. 17. Closed-loop input impedance comparison for two different output power values (Vi=700 V, Ci=14.1 mF, Rcin=0.005 Ω)

As can be seen in the Fig. 17, **the reduced order model is properly adapted to the experimental results obtained for the different powers**.

It can be observed how at low frequencies the controlled converter acts as a constant power load, and how at high frequencies the effect of the parasitic resistance of the input capacitor appears. The model has been modified by finally adding the parasitic resistor (*Rcin*) in series with the input capacitor

5.3 Behaviour with negative current reference *(Grid connection, Current control, DQ)*

In this case, the impedance is checked in the case that the reference current in the controller is modified, setting a negative current in this case, which causes the inverter to change the power direction, extracting power from the grid and injecting it into the DC bus. By definition in this case the input impedance is not being seen, instead the output impedance is being seen.

A negative power has been used instead of a positive one in the reduced order model, in order to check if the impedance behaviour of the system is properly adapted when it acts with the previous conditions.

It can be observed in Fig. 18 how at low frequencies the constant behaviour is maintained, with a difference with respect to the previous cases in the phase, this is due to the fact that in this mode of operation the inverter is behaving as a constant power source.

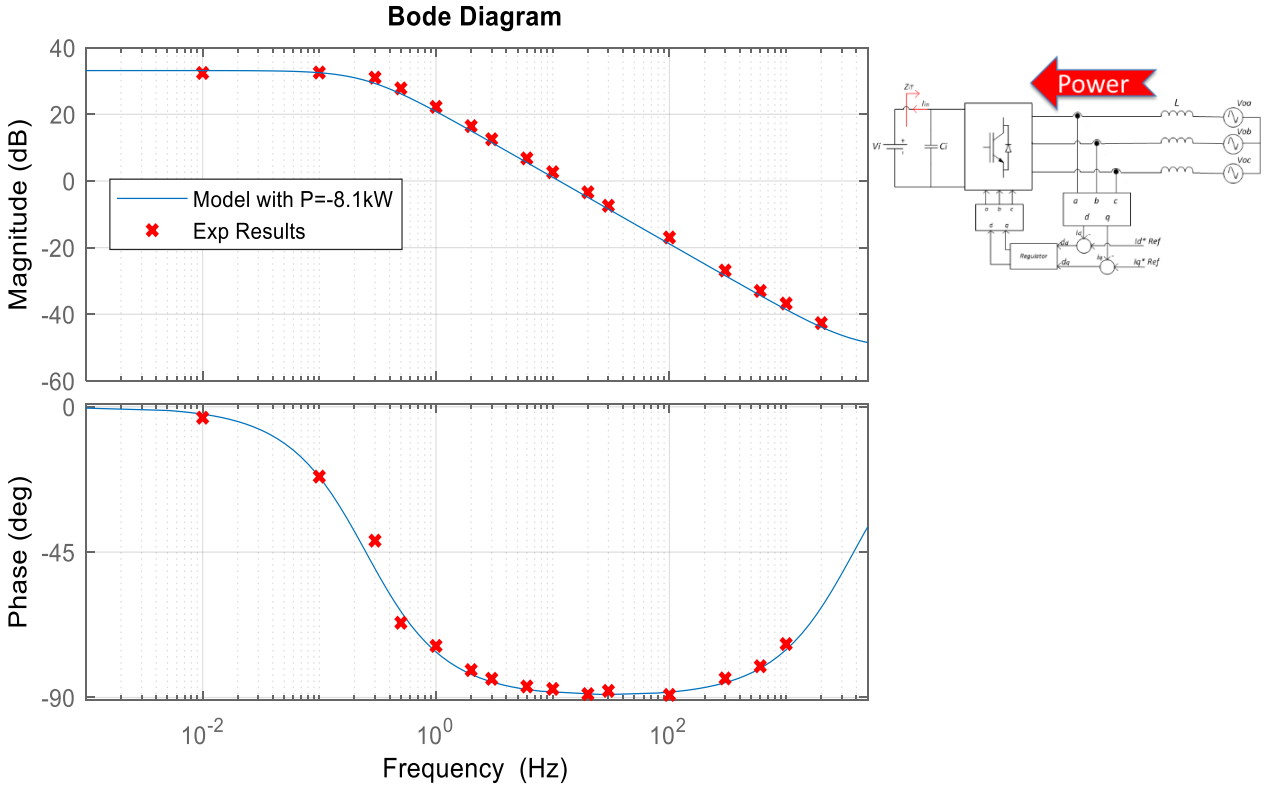

Fig. 18. Closed-loop input impedance with negative current reference value (Vi=700 V, Ci=14.1 mF, Rcin=0.005 Ω, Po= -8.1kW)

This study is very interesting for the system stability, since if a system had an inverter that could act both as load and as source, it would be necessary to know its input impedance when it behaves as load and its output impedance when it behaves as source, from these studies the worst case for stability would be obtained and the rest of the bus would be designed to be stable.

With the study that has been carried out it can be concluded that the model correctly predicts the change in the current reference and therefore can also be used to obtain the output impedance when working on this particular case.

5.4 Behaviour with a resistive load *(Current control, DQ)*

In this case the inverter load has been modified, instead of using an active load, grid connection, a passive load, three-phase resistor bank has been used. In order to carry out this test, the PLL had to be eliminated and the reference angle had to be generated to be followed by the current from an implemented Simulink generator and then loaded into the Opal RT.

This test eliminates the effect of the PLL because the control and elements of the inverter remain the same.
As can be seen in Fig. 19, the model is properly adapted to the experimental results, which means that in this case the PLL does not affect the impedance of the system.

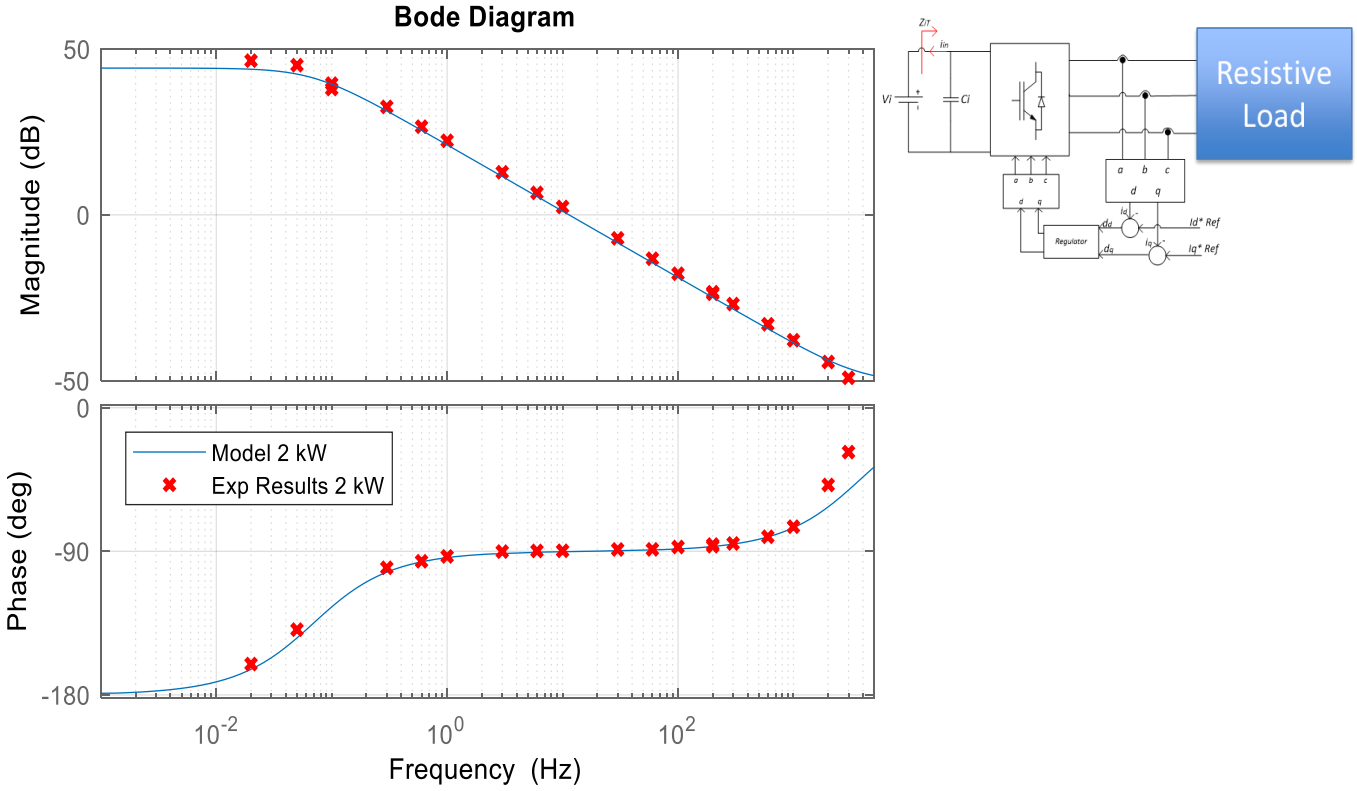

Fig. 19. Closed-loop input impedance when using a resistive load
(Vi=700 V, Ci=14.1 mF, Rcin=0.005 Ω, Po= 2 kW)

5.5 Behaviour with an external control loop *(PQ Control, DQ)*

In this case the control shown in Fig. 6 has been modified, instead of having a constant current reference set manually, the current reference is imposed by an external power controller. This power controller is much slower than the current control.
As can be seen in the Fig. 21, the reduced order model is properly adapted to the experimental results. So, the external PQ control does not directly affect the closed loop input impedance.

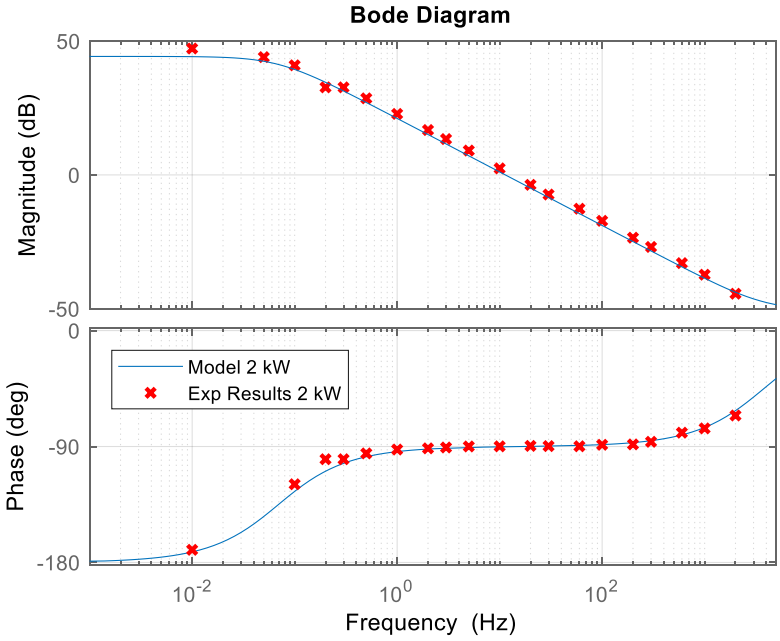

Fig. 20. Closed loop input impedance with an external PQ control.
(Vi=700 V, Ci=14.1 mF, Rcin=0.005 Ω, Po= 2 kW)

5.6 Change in control bandwidth *(Current Control, DQ)*

In the following test different controls have been tested, the time constant τi of the PI controller was modified. this time constant is proportional to the control bandwidth. A time constant of 1 ms was used for the first test. The result of this first test can be seen in the Fig. 23.

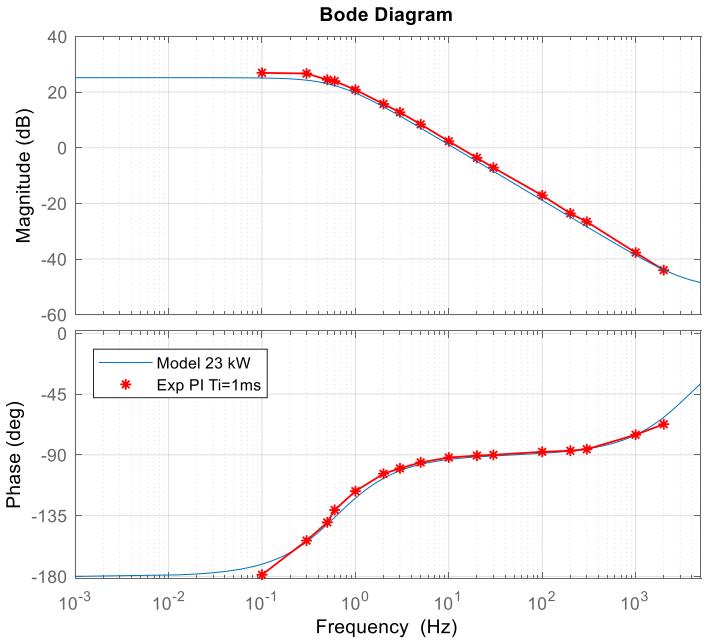

Fig. 21. Closed loop input impedance with a current control using a $\tau i = 1$ ms

(Vi=700 V, Ci=14.1 mF, Rcin=0.005 Ω, Po= 23 kW)

It can be observed how the model fits properly to the experimental results. For the following tests, the control time constant has been changed to $\tau i = 5$ ms

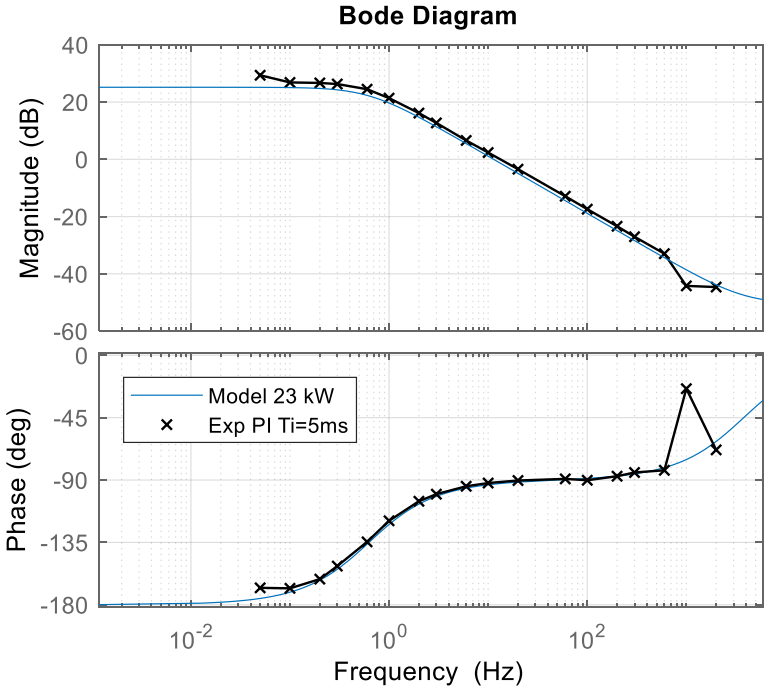

Fig. 22. Closed loop input impedance with a current control using a $\tau i = 5$ ms

(Vi=700 V, Ci=14.1 mF, Rcin=0.005 Ω, Po= 23 kW)

As it can be seen the model still adapts properly, except for some points in which it is believed that the data has not been taken properly.

5.7 Conclusions

As conclusions to the previous studies it can be said that the model fits properly to the closed loop input impedance of the converter in all cases except the last one. Using only a proportional control is not a common practice since normally PI or more complex controls are used. So, although in this case the model does not fit correctly, for the rest of cases it predicts the input impedance with good accuracy.

With regard to the use of this model in the stability analysis, it can be said that although the model has small differences with the real impedance, it can be used perfectly in the stability analysis as long as the stability of the system is not studied in order to have a case of critical instability. Therefore, it will be necessary to take into account and add a certain safety margin at the moment of studying the stability of the system. This margin is already used in the stability studies performed with the analytical results, so the use of this margin is not an inconvenience.

6 Open Issues and Suggestions for Improvements

There are some open issues all of them related to more measures that could add extra value to the stay:

- Input impedance measurement in a controlled inverter with **$\alpha\beta$** reference axes: With this test it will be possible to observe how the impedance is affected by the use of different reference axes, in addition it will be possible to see how the impedance is modified by the use of a resonant proportional control.

- Input impedance measurements in **dq** using a very slow low pass filter applied to the input voltage feedforward: It has been proven in post-stay studies that the fact of applying this filter affects the constant power load behaviour, which would be interesting to test in a real high-power converter.

- Perform input impedance measurements for a **3L-NPC** inverter: With these measures it can be seen if for other topologies the constant power load behaviour is still maintained. In this case more effects of the control loop could be seen since the input capacitor of this converter is usually smaller than the one used in inverters with 2L-VSC topologies.

It would also be interesting to be able to remake the last experiments using different controls, in order to observe if the not corresponding points are due to a bad measure or is the real impedance of the converter.

7 Dissemination Planning

It is planned to prepare different scientific publications in several conferences and journals. As prestigious conferences in the field, we have already submitted some results of the project in conference papers.

One paper has been accepted at SAAEI 2019 and another paper is under review at IECON 2019. In addition, it is also planned to send one paper to be published in prestigious journals in the field like IEEE Trans. on Power Electronics (IF: 7.151), IEEE Trans. on Industrial Electronics (IF: 7.168), IEEE Journal of Emerging and Selected Topics on Power Electronics (IF: 4.269) or Applied Energy (IF: 7.182).

Moreover, a detailed dissemination of all results will be included in the PhD thesis of Daniel Santamargarita.

This research and results are also part of the CONEXPOT project (DPI2017-84572-C2-2-R) (AEI/FEDER, UE), which is a national project comprised of different academic partners with the aim of standardizing the design of the interconnected architectures, in order to develop new methods and tools that can aid in the analysis and design of these systems.

Finally, a reference of the project on the websites of the User Group Institution will be included.

8 References

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9 List of Figures

10 List of Tables