

Testing an IEC 61850-based Light-weighted Controller for Reactive Power Management in Smart Distribution Grids

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Abstract— Due to the large-scale integration of distributed energy resources (DER) new options for the local and system-wide technical ancillary services are needed. Reactive power control is one of such ancillary service provided by DERs. This paper aims to test the performance of a reactive power control scheme developed on a light-weight Intelligent Electronic Device (IED). The IEDs are implemented on a BeagleBoneBlack as well as on an FPGA. The test set-up is implemented by the Controller-Hardware-In-the-Loop platform. The simulation platform is OPAL-RT's eMEGASIM and ePHASORSIM. The results show the performance of the FPGA to be better than BeagleBoneBlack when comparing results of the Software-In-the-Loop simulations.

Keywords—Control Systems, Microgrids, Power system simulation, Testing

I. INTRODUCTION

The electrical distribution systems have grown mainly with the increasing connection of decentralized energy sources and communication between their different components. Numerous studies have been conducted to identify how these components are controlled to support the management of the power grid, based on its real-time operation. In this context, some studies focus on the management of the reactive power capabilities of these sources to support local voltage throughout the distribution system [1] [2] [3] [4] and mainly to comply with reactive power distribution in-feed requirements imposed by grid codes [5]. Since actors are spread across the grid, Information and Communication Technology (ICT) plays a crucial role to coordinate and provide reactive power support. [6].

The latter brings new challenges in determining the performance of the distribution grid when having to consider both power system and communication phenomena and requires rigorous system testing under dynamic conditions [7]. The shift from offline modelling and simulation to hardware in the loop simulation allows the testing of both hardware and software planes under real-time conditions [8]. Techniques such as Controller-Hardware-In the-Loop (CHIL) are topics of research aligned on how these systems can be tested, with the advantage of a good fidelity which helps to study grid behavior of control mechanisms [9] [10] [11]. In CHIL, the hardware controller exchanges low powered analog signals with the real-time simulator. This has the benefit that different operational scenarios can be investigated under controlled experiments without harming any physical system. Also, the hardware controller can be programmed for parameter

adjustment during the run time, which increases the flexibility of the test system and the simulation [12] [13]. Additionally, different communication protocols may be tested in CHIL to find out the optimal information exchange between hardware and software.

IEC 61850 is one of the popular automation protocol, due to the fast and reliable measurement rate provided by GOOSE over the Ethernet. In addition to reliable communication, the system and the controller can be modelled and automated using the IEC 61850 functions which map the measurements on the controller. Although IEC 61850 standards offers many benefits, recent works [14] [15] [16] [17] [18] [19] [20] [21] show that the major challenges facing the implementation of the IEC 61850 standard is the configuration task based on the available IED and system configuration tools within a multivendor environment. The recent works mentioned above are pilot projects that were used in the commercial IEDs in a designed laboratory platform and the commercial software configuration tools. Moreover, the commission task needs system support tools from the manufacturers. Therefore, research and development tasks can be more costly and time-consuming. However, in terms of accelerating research, development and relaxing the IEC 61850 implementations tasks, Light-Weight IEC 61850 IEDs can be used. Various open-source libraries are available that are based on C and Java solutions. These solutions automatically generate the low-level machine code required for the IEC 61850 implementation within different operating systems such as Linux, Windows, and macOS. Embedded open-source operating systems (Linux) running on the microcontroller and SoC kit are becoming increasingly popular in both industrial and academe domain since it is cost-effective and very flexible in its configuration.

This paper aims to present the implementation of a reactive power controller based on light-weight IEDs and test the performance. Section II presents the reactive power algorithm for Sundom Smart Grid. Section III presents the development process of the real-time simulation platform. More details about the Light-Weight IEC 61850 implementation is in section III B. Section IV presents the executed tests and experiments. Section V presents the round trip latency for GOOSE messages with the tested hardware. Finally, the conclusions are presented in Section VI.

II. REACTIVE POWER CONTROL ALGORITHM FOR SUNDOM SMART GRID

An algorithm of reactive power management for future Sundom Smart Grid has been developed by offline simulations in [22], [23]. The case studies and this precursor algorithm has been developed with Simscape Power Systems. In this research, the algorithm is developed further for adapting it to the real-time simulation platform.

A. Sundom Smart Grid

Sundom Smart Grid (SSG) is a unique Smart Grid living laboratory pilot that is established in an MV network. The primary substation and four secondary substations are equipped with modern IEDs, and fiber optic connections are provided to each IED. A cloud service is set up to collect the IEC 61850 sampled values and GOOSE measurements from the network. A direct communication link from the site to the university's Smart Grid laboratory is also set up. The data collection facilities are used in various research activities.

At present SSG is facing challenges with the recently enacted requirements for Reactive Power Window (RPW) settled by the Finnish Transmission System Operator (TSO), Fingrid. RPW specifies the volume of reactive power that can be delivered to and received from the main grid without separate compensation. The output energy is calculated based on the hourly average (Q , P) for the previous 12 months. The fees are set to the points/situation that crosses the limits. A reactive power window for SSG that has been developed in [22] is presented in Fig 1. For this research, a whole year measurement data is available from SSG, and the situation is presented in Fig. 2.

B. Reactive power control

Reactive power management algorithm has been developed in [23] aiming to prevent the fees in SSG, and the paper presents the increasing fees estimated due to the increase in cabling during the years 2018, 2019 and 2020.

In this research, the reactive power window for future SSG [22] is utilized, and the reactive power control of SSG is implemented with the RPW algorithm for a 3.6 MW full-scale wind turbine (WT) converter. The outline of the simulation model is presented in Fig. 3. The RPW controller was developed further from the Simscape (phasor, continuous) model to the Simulink model fitting into the eMEGASIM real-time simulation platform.

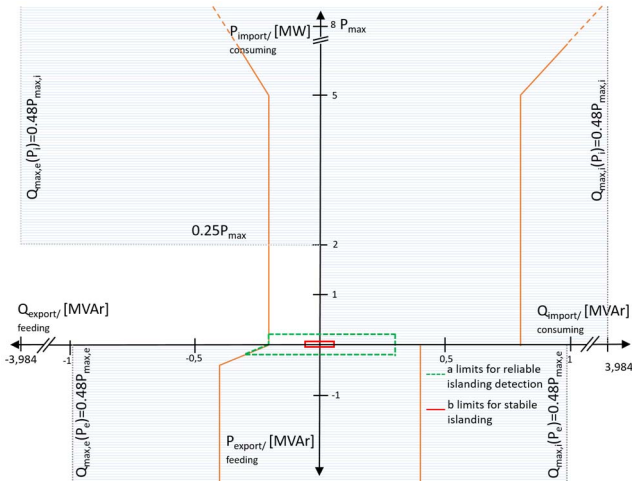


Fig. 1. Active and reactive power operation limits for future SSG. [22]

III. DEVELOPMENT PROCESS OF THE REAL-TIME CO-SIMULATION PLATFORM

The workflow of the development of the real-time co-simulation platform consisted of use case development, offline simulation model development, open-loop simulations, real-time model development and closed-loop simulations offline, IEC61850 communication implementation, the SIL tests as well as the CHIL tests. In the following, this development process is described in more details.

In the first phase, different use cases were developed about the evolving SSG for investigating the operation of the power system and validating it according to the measurements. After that, the RPW controller was developed. In the previous research [22] [23], the reactive power control has been implemented as an open-loop i.e. the first simulation results (control values) were the input to the second round and fed in to the RPW controller. This method was used because the direct closed-loop simulations did increase the simulation time greatly. The SSG and the controllers have been modeled in that case by Simscape in phasor mode.

The results from the Simscape simulations showed the behavior of the power grid, which makes it possible to evaluate further the other interesting use cases for the real-time simulations. For the real-time modeling, particularly for the ePHASORSIM (the power system model) block, it was possible to import simulation models of the offline tools. The offline models were modeled and verified in PowerFactory and then converted to real-time models for ePHASORSIM simulation.

Based on Simscape results, the interesting use cases and the interesting moment of them (interesting hour) were selected to give the initial values of loads and generation as well as the voltage at the HV connection point for the PowerFactory model.

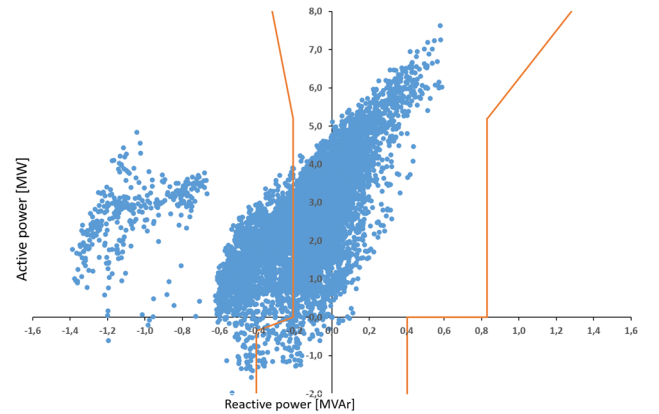


Fig. 2. Measured hourly active power as a function of measured reactive power in the TSO's reactive power window for the SSG.

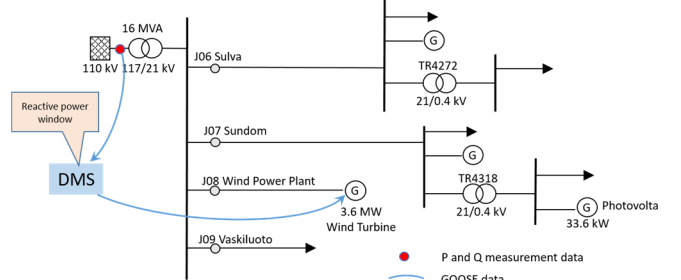


Fig. 3. Outline of the simulation model. [24]

A. Development of the real-time models

For the development of the real-time simulation model, the generated Excel file was imported into the ePHASORSIM block in the eMEGASIM model in OP5600 platform of OPAL-RT. The structure of the resulting model is outlined in Fig 4.

Further, the developed control algorithm, as well as the load (P_{load}) and the generation ($P_{\text{generation}}$) data from the Simscape blocks, were also imported to the eMEGASIM. After the real-time models for the basic cases Status 2018 Scenario 2028, as well as Scenario 2035, were built-up, the offline simulations by the real-time models were very efficiently performed for the one-year load flows compared to the Simscape simulations. For example simulating offline one year power flow (in phasor mode) of the basic case Status 2018 with processor Intel Xeon CPU E3-1505M v6 @ 3.00 GHz and installed RAM 32 GB took minimum 6 min (no scopes, no data to workbench) and maximum 14 min (with scopes and data to workbench) to perform the simulation with Simscape (variable step), Matlab r2017a and about 30 s with ePHASORSIM, Matlab r2015a respectively. Fig. 5 and 6 present offline results of RPW in the case Status 2018 with Simscape and ePHASORSIM, respectively. It can be noticed that the results of the offline simulations by the real-time models were consistent with the results from Simscape and hence to PowerFactory results.

Next, after the real-time models of the basic network structures were built up and working well, the RPW controller was tuned for the closed-loop simulations. The offline simulations were carried out after the controller was found to be working well. The closed-loop offline simulations for Scenario 2018 (RPW control) with ePHASORSIM, based on Matlab r2017a took about 6 min when several scopes, data to the workbench and average calculation blocks were applied, while Simscape open-loop simulations took 15 min + 15 min as previously explained. Further, when the real-time models were running well in offline mode, it was time to run the models in real-time. The results were consistent with the offline simulation results.

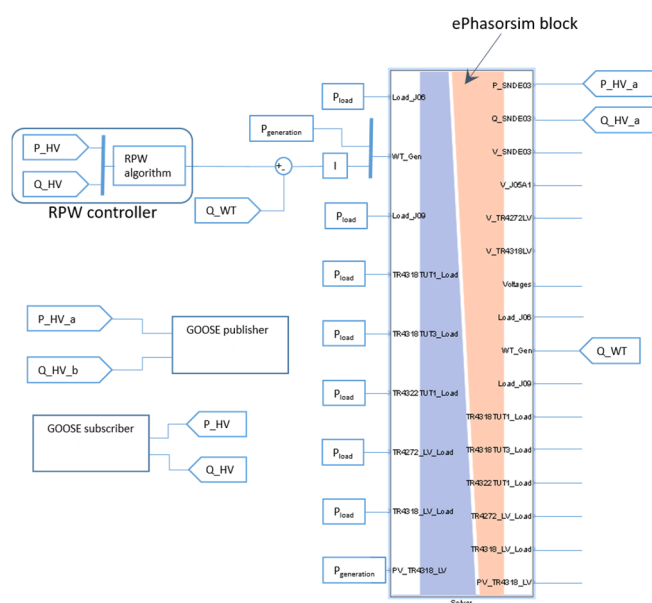


Fig. 4. The simulation architecture in SM_block for SIL of reactive power control in SSG Status 2018. [24]

After the real-time models were running well, the implementation of the communications to the real-time model for the SIL and the CHIL tests was the next phase. The IEC61850 GOOSE was implemented for sending the active power and reactive power measurement values (P_{meas} , Q_{meas}) from the point of interconnection to the RPW controller. This real-time co-simulation platform is presented in Fig. 7. Fig. 4 shows the GOOSE publisher block that was implemented in the real-time model for publishing (sending) the P and Q values from the target (OP5600 simulator), as well as the GOOSE subscriber block that was implemented for subscribing (receiving) the P and Q values from the Ethernet network.

In SIL case, the GOOSE publisher, as well as the subscriber block, were inside the model. For the publisher and the subscriber GOOSE blocks, one configuration file (*.icd) was developed by IEC 61850 ICD Designer tool that is a

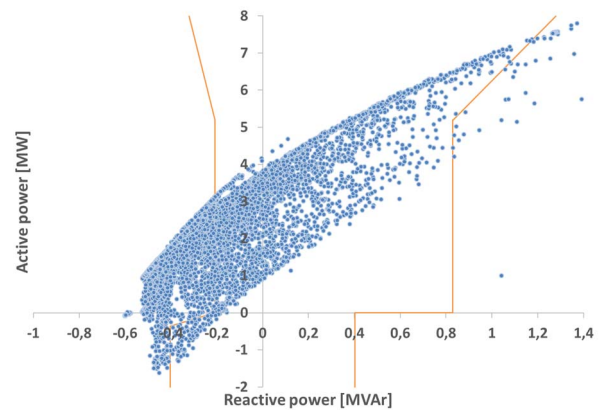


Fig. 5. RPW of the Status 2018 with Simscape.

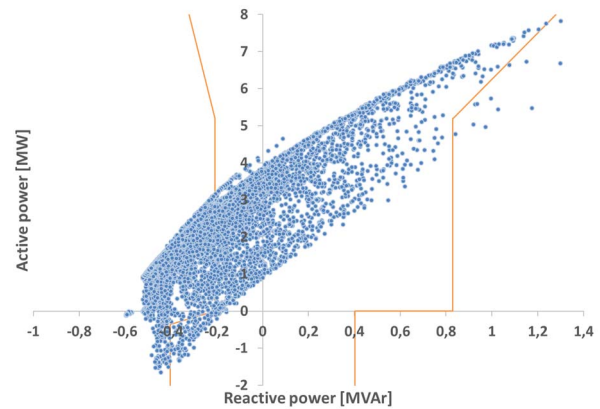


Fig. 6. RPW of the Status 2018 with ePHASORSIM.

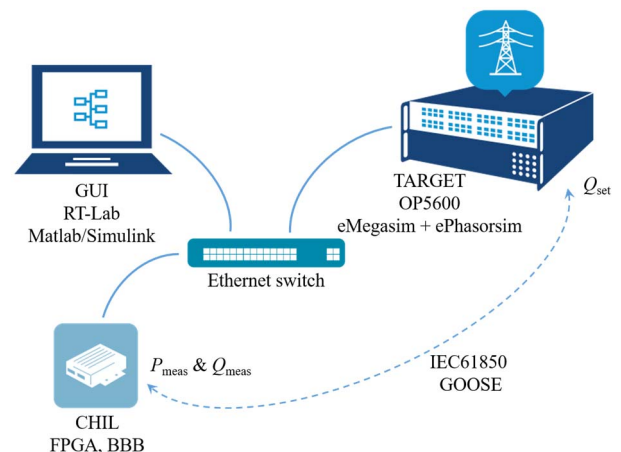


Fig. 7. The real-time co-simulation platform. [24]

software for configuring and modeling IEC 61850 clients and servers. The configuration file was created using a suitable set of Logical Devices (LDs) and Logical Nodes (LNs).

B. Implementation of the developed RPW control algorithm in controller hardware

Further, for the CHIL simulations, the Substation Configuration Description (SCD) file was developed and further adapted into two different hardware, namely to the BeagleBone Black (BBB) and the Field Programmable Gate Array (FPGA). The following paragraphs present implementation phases of the control algorithm to the hardware, where the developed C++ code included the RPW control algorithm, the GOOSE publisher and subscriber.

A “lightweight” implementation of IEC 61850-8-1 (mapping the IED data to GOOSE) that was done offered a practical approach for the CHIL by using the open-source library “libiec61850”. Furthermore, the designed controller generated by this process can communicate with other IEC 61850 IEDs. The developed controller is flexible, and the files from the project C code can be generated from any valid SCD file. The generated C code files define the internal data model of an IED. This approach maximizes runtime performance and facilitates the use of relatively low-cost embedded devices and FPGA.

The procedure for designing the “lightweight” controller is presented in Fig. 8. In this study, the first step was designing an SCD (.icd) file that included the Logical Node (LN), data object (DO), and Data Attribute (DA) types as well as communication instances of the model.

For the second step, a C code representation of a model and their communication instances that are tailored to this model was automatically generated from the designed SCD file by the “libiec61850 model generator”. According to the “model generator” process, each type of IED data model can be mapped directly to a C data structure, resulting in a hierarchy of C data structures. Besides, the generated C files must be accompanied by the platform-specific code to ensure consistency with IEC 61850.

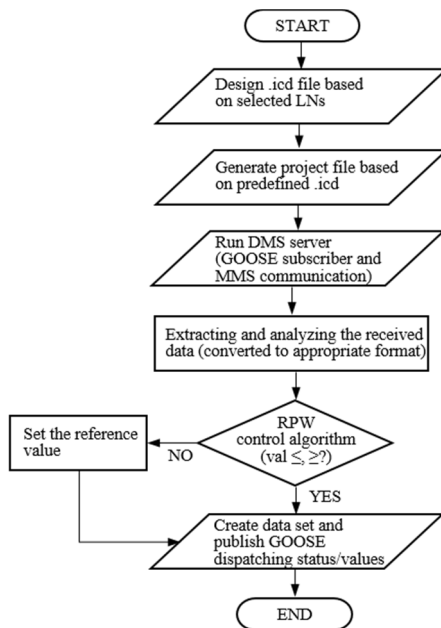


Fig. 8. The developed DMS internal processing. Applied from [25].

The third step was to define the parameters that are needed to be subscribed (in this case P_{meas} and Q_{meas}). Then to compile the design project file (or application file) to generate the execution file for running the project in the hardware under test.

The fourth step was about extracting the defined parameters (in this case P_{meas} and Q_{meas}) from the subscribing GOOSE message from the model. Next step describes the execution of the control algorithm in the hardware and based on the result, the new setpoint value (in this case Q_{set}) is published from the hardware under test back to the target (simulation model) via GOOSE.

The project was tested by the Advanced RISC Machines (ARM) processor-based microcontroller BBB as well as by the ARM processor-based SoC FPGA where both processor and FPGA architectures are integrated into a single device. Both are compatible with C and C++ compilers.

IV. EXECUTED TESTS AND EXPERIMENTS

For the real-time SIL and CHIL simulations, the simulation time step (T_s) was 0.01 s. The time factor (T_d) for reading data row from the input data (1 h average values) or the look-up table was set 0.1 s hence corresponding one-hour data. The data gathered to the real-time target were P_{HVavg} , Q_{HVavg} , P_{HV} , Q_{HV} , P_{WT} , Q_{WT} and the voltages 110 kV, 21 kV and 400 V. The CHIL tests were performed for the BBB as well as for the FPGA controller. From the IEC 61850 GOOSE messages, the packets traveling over the network were captured by Wireshark software that created .pcap files from the traffic between the controller in the test and the target.

A. Scenario 2018 with RPW control in SIL

In this case, Q_{set} for the RPW controller was according to the TSO limits ± 50 kVar, except $Q_{D1} = -200$ kVar. The reactive power of the WT converter is presented in Fig. 9 showing both the SIL offline and the real-time results.

When comparing the real-time results with the offline simulations, it can be noticed that there are slight differences in the controlled values. This is because of the delay from the communications that is obvious with real connections. The T_d factor was set tight to show the characteristics of the different hardware. However, in this study, one simulation step (10 ms) delay would represent 360 s delay in the real world.

B. Scenario 2018 with RPW control in CHIL

The comparison in Scenario 2018 was made between SIL real-time simulations, BBB, and FPGA. Fig. 10 presents the reactive power flow from the WT converter when $T_d = 0.1$. The comparison is made between SIL and BBB, between SIL and FPGA as well as between BBB and FPGA. In every case, differences can be noticed. This happened due to the different processing times of the hardware, which effect is presented in more detail in Fig. 11. After the first simulated hour, it can be noticed that the Q_{WT} have different values. The SIL controller calculates a new set value for the WT converter in every 10 ms (at the same time with the simulation time step) for the controller. The CHIL controller, in turn, calculates a new set point that is delayed with the round trip time, i.e. communication delays in Ethernet and processor calculation time step. This is analyzed in detail in section V.

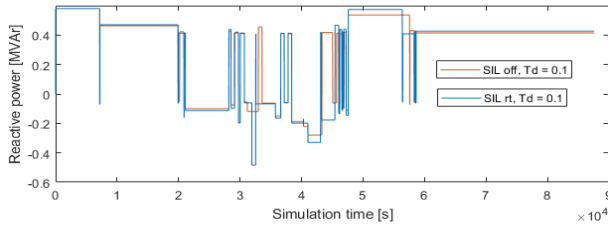


Fig. 9. SIL offline and SIL real-time simulation of the Scenario 2018. Reactive power of WT when $T_d = 0.1$. The RPW controller was set up to the TSO limits ± 50 kVar, except $Q_{D1} = 200$ kVar.

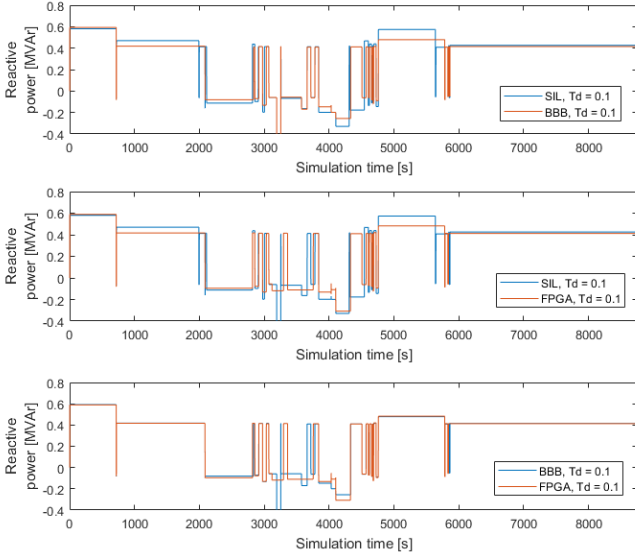


Fig. 10. Comparison of SIL real-time and CHIL test results in Scenario 2018/2. Reactive power of WT when $T_d = 0.1$. The RPW controller was set up to the TSO limits ± 50 kVar, except $Q_{D1} = 200$ kVar.

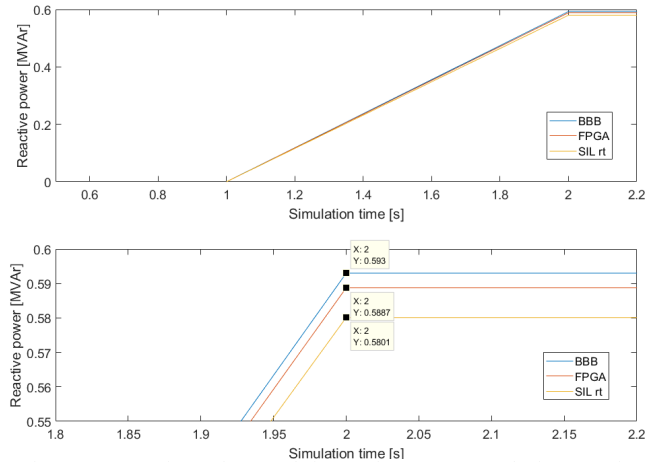


Fig. 11. Comparison of SIL real-time and CHIL test results in Scenario 2018. Reactive power of the WT.

V. THE ROUND TRIP GOOSE LATENCY

The round trip GOOSE latency was calculated for the overall completed tests. The main objective within this measuring task was to verify that the performance of the Device Under Test (DUT) for the publishing of the GOOSE messages was compliant with the IEC 61850 (not exceed 4ms). Moreover, to verify that the DUT had the ability to operate within the multi-vendor environment ensuring the interoperability concept.

For comparison of the round trip time of different devices, the instantaneous GOOSE round trip latency was measured for the tested lightweight IEDs. The GOOSE round trip

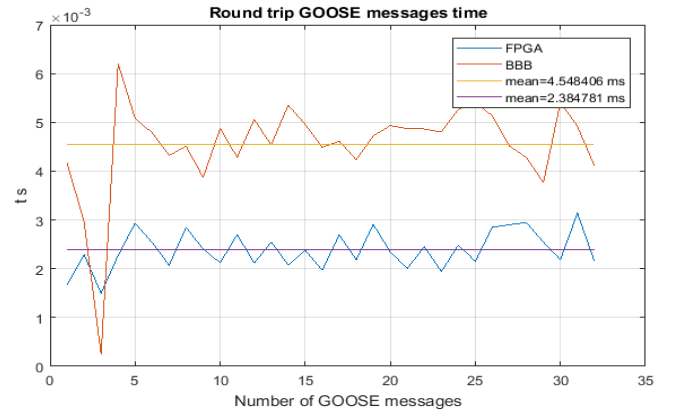


Fig. 12. The round trip GOOSE latency of BBB and FPGA.

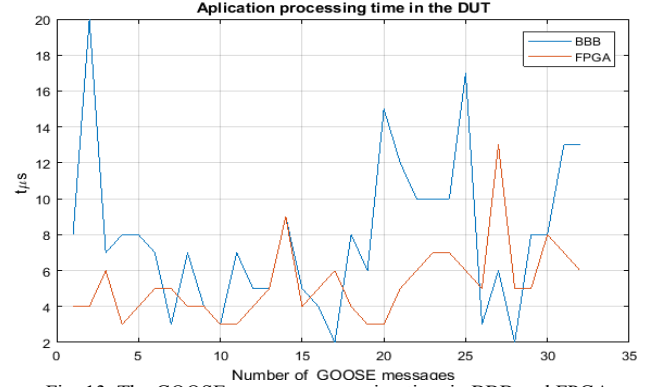


Fig. 13. The GOOSE message processing time in BBB and FPGA.

latency time includes seven individual times that may affect the connection channel performance as illustrated in (1). It starts from the real-time model running in the target that publishes GOOSE messages (Q_{HV} and P_{HV}), next there is the DUT that subscribes the message, computes the Q_{set} based on the RPW algorithm and then periodically publishes a GOOSE message containing magnitude Q_{set} for the simulated WT converter. This process was monitored by using a network protocol analyzer, Wireshark.

$$\bar{t}_{RTT} = \bar{t}_{out, Target} + \bar{t}_{net} + \bar{t}_{in, DUT} + \bar{t}_{app} + \bar{t}_{out, DUT} + \bar{t}_{net} + \bar{t}_{in, Target} \quad (1)$$

where

\bar{t}_{RTT} the average round trip time,
 $\bar{t}_{out, Target}$ the average time out from the target (client IED),
 \bar{t}_{net} the average time in Ethernet network,
 $\bar{t}_{in, DUT}$ the average time in to the DUT,
 \bar{t}_{app} the application average time running on the DUT,
 $\bar{t}_{out, DUT}$ the average time out from the DUT,
 $\bar{t}_{out, Target}$ the average time in to the target

Fig. 12 presents the round trip GOOSE latency for the BBB and the FPGA. Average round trip latency calculation based on (1) was 4.548406 ms for BBB and 2.384781 ms for FPGA. Based on the results, it is clear that the FPGA is a more promising instrument with less round trip latency (2.3 ms) that could be used for the smart grid or microgrid central controller. It was expected that the round trip latency would be less for the FPGA since it has Dual-Core ARM Cortex™.

A9 (925 MHz) processor as well as 10/100/1000 Mbps Ethernet with the high-speed bus to exchange data between the hard processor system (HPS) and FPGA whereas the BBB has AM335x 1GHz ARM® Cortex-A8, and 10/100 Mbps Ethernet. Fig. 13 presents the GOOSE messages processing time in both devices.

VI. CONCLUSION

In this paper, the performance of the reactive power control scheme developed on a light weighted intelligent electronic device has been investigated. The control solution and its relevant communication system have been designed based on IEC 61850 and implemented on two hardware platforms, FPGA and BBB. The performance of the IEDs has been evaluated through Controller-hardware-in-the-loop versus software-in-the-loop test in terms of communication latency, processing time, and finally, the performance of control action. The FPGA has performed better compared to BeagleBonBlack and is more suitable for a micro-grid central controller. It is worthwhile to mention that such an open-source flexible light-weighted IED based on IEC 61850 can provide a base to advance research in the direction of (Micro)-grid automation and control.

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